K 1223

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2004.

Third Semester

Information Technology

IF 245 — COMPUTER ARCHITECTURE

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. State any two issues to be considered while encoding an instruction format.

2. State any two addressing modes followed in RISC processors and explain them with suitable examples.

3. Give the IEEE standard format for a double precision floating point number and explain the various fields.

4. What is a write buffer? How is it useful?

5. What is the principle of operation of a carry–look–ahead adder?

6. What is a TLB? What is its significance?

7. What is meant by memory interleaving?

8. State different ways of achieving parallelism in uniprocessor systems.

9. What is the ideal speedup of a pipeline with m stages? State the assumptions made.

10. What is meant by space level redundancy and time level redundancy?

PART B — (5 × 16 = 80 marks)

11. (i) What are the different types of hazards that can occur in a pipeline? How can each of them be minimized/overcome? Discuss. (10)

(ii) Assume that a program has the following instruction mix :

Instruction type	Frequency	Clock cycle count
Fixed point ALU operations	40%	1
Loads/Stores	20%	3
Branches	30%	2
Floating point operations	10%	4

Calculate the CPI and the MIPS rating for a processor operating at 500 MHz. (6)

12. (a) (i) Give the general organisation of a hardwired control unit and explain how an instruction gets executed here. (10)

(ii) Discuss the Booth's multiplication algorithm. Give the Booth's multiplier for 1100110101111. (6)

Or

(b) (i) Discuss any one binary division algorithm. Simulate the same for $33 \div 8$. (10)

(ii) What is a microprogram sequencer? What is its functionality? (6)

13. (a) (i) Draw the basic cell of an associative memory unit. Show how an $m \times n$ memory is constructed using this basic cell. (10)

(ii) Discuss the relative advantages and disadvantages of the three mapping techniques used in cache memories. (6)

Or

(b) (i) What is a DMA transfer? How does it take place? (10)

(ii) Write a short note on the functionalities carried out by an I/O processor. (6)

14. (a) (i) Discuss the Flynn's architectural classification scheme, bringing out the salient features of each of these types. (8)

(ii) What is an arithmetic pipeline? Explain with respect to a floating point unit. (8)

Or

(b) (i) What are vector processors? Discuss their design issues. (8)

(ii) What are the different types of multiprocessor systems? Discuss. (8)

15. (a) Discuss the salient features of a typical RISC processor like SPARC.

Or

(b) (i) What are data flow processors? Discuss their merits. (8)

(ii) What are the different ways in which redundancy can be applied to a system? Define the performance metrics associated with fault tolerance. (8)

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