

S 9112

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2006.

Third Semester

Mechatronics Engineering

EC 154 — DIGITAL ELECTRONICS

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

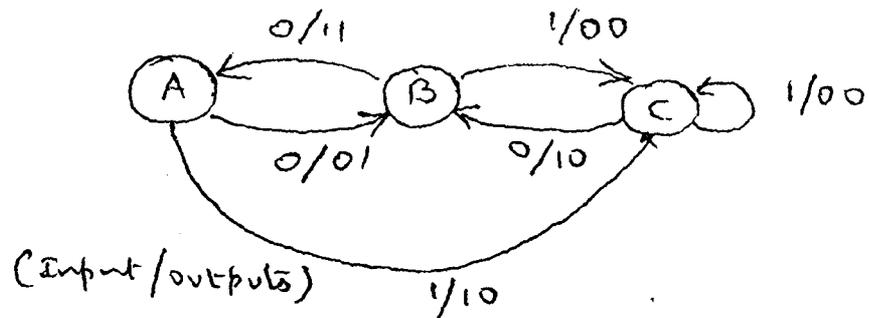
1. What are alphanumeric codes? Give two examples.
2. Perform 2s complement subtraction : 1100 – 1100011.
3. Implement full adder using two half adders and an OR gate.
4. Distinguish between PAL and PLA.
5. What are the states possible in a 3-bit Johnson counter?
6. Write the excitation table of JK FF.
7. What are the assumptions in forming primitive flow tables?
8. Define dynamic hazard.
9. What are the three basic components of an ASM chart?
10. Define state locus.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Obtain ASM chart for a mod-8 binary up-down counter. (10)
(ii) Explain transition and stable periods using the timing diagram of a general algorithmic state machine. (6)

Or

- (b) (i) Draw the ASM chart for the following state diagram : (10)



- (ii) Explain the difference between state diagrams and ASM charts. (6)
12. (a) Obtain simplified SOP using Tabulation method

$$F(w, x, y, z) = \Pi(0, 1, 2, 3, 4, 10, 11)$$

Or

- (b) (i) Perform BCD addition of 295_{10} and 157_{10} . (8)
- (ii) Using K-map obtain simplified POS for
- $$f(a, b, c, d, e) = \Pi(0, 2, 4, 6, 9, 11, 13, 15, 17, 21, 25, 27, 29, 31). \quad (8)$$
13. (a) Design a 4-bit magnitude comparator and give its logic diagram.

Or

- (b) (i) Design a BCD adder. (10)
- (ii) Realize a 2 digit BCD adder. Use block diagrams. (6)
14. (a) Design a counter for the binary sequence 0, 1, 3, 7, 6, 4 and repeat. Use T FFs. Use don't cares for unspecified states.

Or

- (b) (i) Explain the working of a basic IC memory cell and show the logical construction of an IC RAM of 4 words of 3 bits each.
- (ii) Write the difference between static memory and dynamic memory.

10)

- (a) Explain critical and non-critical races with examples.

Or

- (b) Obtain the reduced primitive flow table for an asynchronous seq. circuit that has two inputs (J and K) and one output (Q). The circuit works as a JK FF. Assume that $Q = 0$ initially.
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6)

3)

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