T 8258

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2006.

Third Semester

Mechatronics Engineering

MH 1201 — DIGITAL ELECTRONICS

(Regulation 2004)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Convert the following :

   (a) $(220.515)_{10} = (\quad)_8$

   (b) $(101010 \cdot 11)_2 = (\quad)_{10}$.

2. Prove that $x + x\,y = x$.

3. Draw a logic circuit to implement the function of EX–OR gate only using any one of the universal gate.

4. Differentiate between PAL and PLA.

5. What is meant by race around condition? How it is avoided?

6. What is lock out? How it is avoided?

7. What is meant by a hazards?

8. Draw a general structure of an asynchronous sequential circuit using delay elements.

9. Name and specify the functions of basic components in the design of ASM charts.

10. Give a sample structure of a PLA realization for an ASM.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Convert the following number system into another number system : (4)

(1) $(25 \cdot 25)_{10} = (\quad)_2$

(2) $(50 \cdot 25)_{10} = (\quad)_8$

(3) $(36 \cdot 24)_8 = (\quad)_2$

(4) $(F3 \cdot BD)_{16} = (\quad)_2$.

(ii) Perform the following subtraction using 1's and 2's complement method. (8)

(1) $(11010)_2 - (10000)_2$

(2) $(1000100)_2 - (1010100)_2$.

(iii) Implement the following Boolean function with NOR gates : (4)

$F = A(B + CD) + B\overline{C}$.

Or

(b) Simplify the following function :

$F(a, b, c, d) = \Sigma m(0, 2, 3, 6, 7, 8, 10, 11, 14, 15)$ in sum of products form and realize it using NAND gates only. Also implement the same using product of sum form and realize it using NOR gates. (16)

12. (a) (i) Design a full subtractor circuit only using NOR gates. (8)

(ii) Implement the following boolean expression using ROM : (8)

$F_1(A, B, C) = \Sigma m(0, 2, 4, 7)$

$F_2(A, B, C) = \Sigma m(1, 3, 5, 7)$

Or

(b) (i) Design the full adder circuit using decoder and demultiplexer. (8)

(ii) Design a 3 bit comparator using gates. (8)

13. (a) (i) Draw the truth table and explain the working of RS and JK flip-flops. (8)

(ii) Draw the diagram of 4 bit asynchronous decade counter and explain its working. (8)

Or

(b) (i) Draw the truth table, timing signals and of D flip flop and master slave JK–flip flops. Also explain its working. (8)

(ii) Explain the operation of 4 bit bidirectional shift register with the help of neat diagram. Discuss one application of it. (8)

14. (a) Design an asynchronous sequential circuit that has two inputs X_2 and X_1 and one output Z. When $X_1 = 0$, the output Z is 0. The first change in X_2 that occurs while X_1 is 1 will cause output Z to be 1. The output Z will remain 1 until X_1 returns to 0. (16)

Or

(b) (i) Explain the function of pulsed mode asynchronous sequential circuit. (8)

(ii) For a given boolean function obtain the hazard free circuit. (8)

$F(A, B, C, D) = \Sigma m(1, 3, 6, 7, 13, 15)$.

15. (a) For the ASM chart given, obtain the discrete gate realization with clocked D flip-flops. (16)

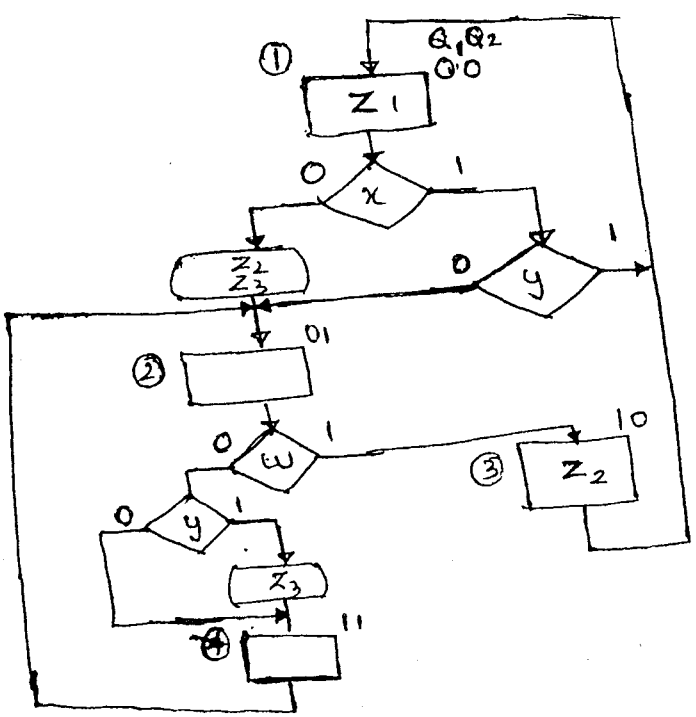

Fig. Q. 15 (a)

Or

(b) For the ASM chart given, obtain the output expression for a PLA realization with clocked D flip-flops. (16)

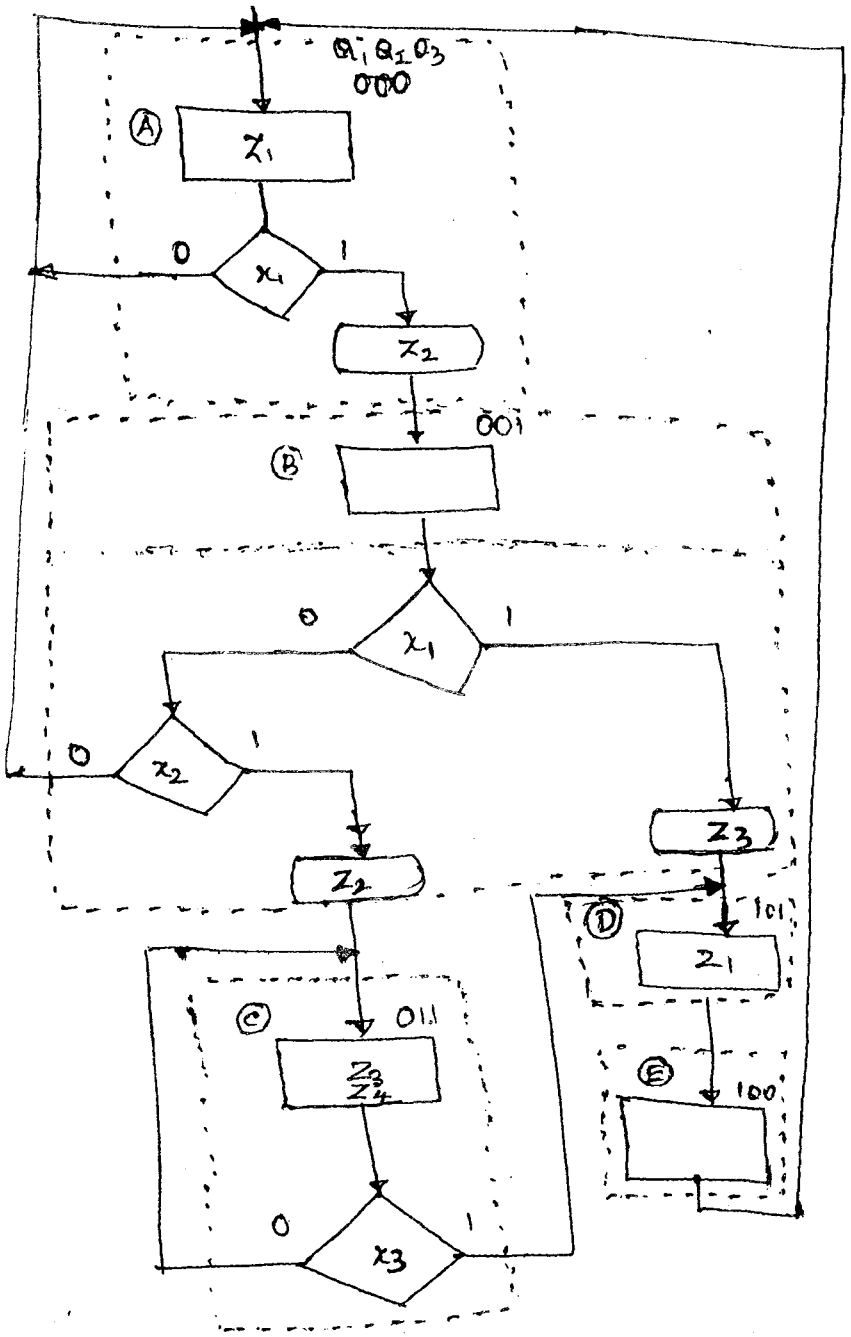

Fig. Q. 15 (b)