

J 1116

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2006.

Third Semester

Computer Science and Engineering

CS 232 — DIGITAL SYSTEMS

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Find the hexadecimal equivalent of the octal number 1024.77.
2. Express $x_1 + x_2 x_3$ as the product of maxterms.
3. Define fan-in and fan-out of a logic gate.
4. Write down the truth table of a half subtractor.
5. Using a SR flip-flop, explain how a JK flip-flop can be built.
6. State the relative merits of series and parallel counters.
7. When is a counter said to suffer from lockout?
8. Distinguish between synchronous and asynchronous sequential logic circuits.
9. State Unger's theorem pertaining to essential hazards.
10. How are ASM charts useful?

PART B — (5 × 16 = 80 marks)

11. (i) State and prove De Morgan's theorem. (4)
- (ii) Using a Karnaugh map, determine the MSP and MPS forms of the switching function

$$F = \Sigma (0, 3, 4, 7, 8, 9, 15) + \Sigma_{\phi} (2, 5). \quad (12)$$

12. (a) (i) Show that the Excess-3 code is self complementing. (6)
(ii) Show that if a weighted code is self-complementing, then the algebraic sum of the weights equals nine. (10)

Or

- (b) (i) Show that the NAND gate is a universal building block. (4)
(ii) Implement a full adder using only NOR gates. (12)
13. (a) (i) State the important features of iterative networks. (6)
(ii) Draw a diode ROM which translates from BCD 8421 to Gray code. (10)

Or

- (b) (i) Implement the following switching function using an 8 input multiplexer

$$F = \Sigma(0, 7, 11, 15) + \Sigma_{\phi}(2, 3, 4, 13).$$
 (6)
(ii) Derive the PLA implementation of a serial binary adder. (10)
14. (a) (i) Derive the characteristic equation of a T flip-flop. (6)
(ii) Using D flip-flops, design a synchronous counter which counts in the following sequence : 111, 000, 110, 001, 110, 111,

Or

- (b) (i) When is a sequential machine said to be strongly connected? (3)
(ii) Minimise the following state table : (13)

PS	NS, Z			
	x_1	x_2		
	00	01	11	10
A	A,0	C,1	F,0	G,1
B	B,0	D,1	F,0	H,1
C	C,0	G,0	H,0	F,1
D	D,0	A,0	B,0	F,1
E	E,0	B,0	H,0	F,1
F	F,0	E,1	A,1	H,0
G	G,0	E,1	F,0	B,1
H	H,0	D,1	F,0	A,1

(6)
g, then the
(10)

(a) Illustrate the technique of hazard free realisation, hazard determination and elimination. (16)

Or

(4)
(12)

(b) (i) Derive the SM chart for a binary multiplier and divider. (8)

(ii) Show that no static 0 hazard can occur in a two level AND-OR realisation of a switching function. (8)

(6)
Gray code.
(10)

8 input

(6)
(10)
(6)

counts in
(10)

(3)
(13)