H 1189

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2006.

Fourth Semester

Computer Science and Engineering

CS 238 — COMPUTER ARCHITECTURE — I

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. State and explain the CPU performance equation.

2. Registers R1 and R2 of a computer contain the decimal values 1200 and 4600.

   Indicate the addressing mode and find the effective address of the memory operand in each of the following instructions :

   Move 20 (R1), R5

   Load # 3000, R5

   Store R5, 30 (R1) (R2)

   Add – (R2), R5

3. Discuss the principle of operation of a carry-save adder.

4. What are the advantages of the Booth's multiplication technique?

5. What are the relative merits of horizontal and vertical microinstruction formats?

6. Consider an unpipelined machine that has 10 ns clock cycles and uses four cycles for ALU operations and branches and five cycles for memory operations. Assume that the relative frequencies of these operations are 40%, 20% and 40% respectively. Suppose that due to clock skew and setup, pipelining the machine adds 1 ns of overhead to the clock. Ignoring any latency impact, how much speedup in the instruction execution rate will we gain from a pipeline?

7. What is a TLB? How is it useful?

8. Write down the expression for the average memory access time for a system with three levels of caches with hit ratios h1, h2 and h3 and access times tc1, tc2, tc3 and main memory access time tm. Explain the same.

9. Distinguish between memory mapped I/O and I/O mapped I/O.

10. Consider a computer in which several devices are connected to a common interrupt request line. Explain how you would arrange for interrupts from device *j* to be accepted before the execution of the interrupt service routine for device *i* is completed. Comment in particular on the times at which interrupts must be enabled and disabled at various points in the system.

PART B — (5 × 16 = 80 marks)

11. (i) Write the sequence of control steps required for the single bus organization for executing the following instruction :

MUL (RO)+, R1, R2, where the first two are source operands and the third is the destination operand. Assume the instruction itself is only a one-word instruction. (8)

(ii) What are the drawbacks of the single bus organization? Show how the multi-bus organization overcomes them. (8)

12. (a) (i) Discuss the principle of operation of carry-look ahead adders. (8)

(ii) Discuss the restoring division algorithm. (8)

Or

(b) (i) Multiply the following pair of signed 2's complement numbers using the Booth's algorithm :

Multiplicand = 010111 and multiplier = 110110 (8)

(ii) Consider a 16-bit, floating-point number with a 6-bit exponent and a 9-bit fractional mantissa where the base is 2 and the exponent is represented in excess-31 format.

Add the nos. A and B, formatted as follows :

A = 0100001 111111110

B = 0011111 001010101

Give the answer in the normalized form. Use rounding to get the 9-bit mantissa. (8)

13. (a) What is meant by a microprogrammed control unit? Give the organization of a typical microprogrammed control unit and explain the functions performed by the various blocks. Critically compare it with a hardwired control unit.

Or

(b) Discuss the concept of pipelining. What is the ideal speedup in a pipelined organization? Discuss the various factors that might reduce the speedup and suggest ways of overcoming / minimizing them.

14. (a) A computer system has a main memory consisting of 1M 16-bit words. It also has a 4K-word cache organized in the block-set-associative manner, with 4 blocks per set and 64 words per block.

- Calculate the number of bits in each of the TAG, SET and WORD fields of the main memory address format.
- Assume that the cache is initially empty. Suppose that the processor fetches 4352 words from locations 0, 1, 2, ···, 4351 , in that order. It then repeats this fetch sequence nine more times. If the cache is 10 times faster than the main memory, estimate the improvement factor resulting from the use of the cache. Assume that the LRU algorithm is used for block replacement.

Or

(b) Explain the concept of virtual memory. Discuss the same for a paged memory management technique.

15. (a) (i) What are the functions to be performed by a typical I/O interface?(4)

(ii) Explain how a DMA transfer is accomplished in a computer system and discuss its relative merits and demerits. (12)

Or

(b) (i) Distinguish between synchronous and asynchronous bus transfers. (8)

(ii) Discuss the storing, organization and accessing of data in a magnetic hard disk. (8)
