H 1196

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2006.

Sixth Semester

Computer Science and Engineering

CS 340 — COMPUTER ARCHITECTURE — II

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Compare CISC and RISC.

2. List out the fundamentals of computer design.

3. What is Pipelining?

4. Mention the merits of dynamic scheduling.

5. Define Speculation.

6. Bring out the applications of super scalar processors.

7. How to achieve synchronization?

8. What do you mean by cache coherence?

9. Mention any 2 bus standards with their applications.

10. List out the importance of Data Flow Systems.

PART B — (5 × 16 = 80 marks)

11. (i) Describe the Architecture of RISC with its block diagram. (6)

(ii) What are the various performance related issues and the parameters? How they can be used for measuring the performance? Explain with suitable example. (10)

12. (a) (i) Explain the instruction pipelining with help of block diagram.

(ii) Describe the various pipeline hazards with suitable example

Or

(b) (i) What is parallelism? Explain the concepts of parallelism.

(ii) With suitable example describe the instruction set architectu design.

13. (a) (i) How to extract the parallelism? Explain the methods of extracti the parallelism with an example.

(ii) Why VLIW? Explain the architecture comparison between CIS RISC and VLIW.

Or

(b) (i) Explain super scalar RISC system in detail with its block diagram. (8)

(ii) Write short notes on vector processors. (8)

14. (a) Describe the following :

(i) Centralised shared memory architecture. (8)

(ii) Distributed shared memory architecture. (8)

Or

(b) (i) What are the various important issues in memory organization? Explain each of them with an example. (8)

(ii) Explain Cache coherence issues in detail with suitable examples. (8)

15. (a) (i) What is SCSI? Explain the uses and applications of SCSI. (8)

(ii) Explain the stack processor with its block diagram. (8)

Or

(b) (i) Write short notes on IO issues and Bus standards. (8)

(ii) Explain the functions of RISC processor. (8)
