L 1055

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2006.

Fourth Semester

Computer Science and Engineering

CS 1251 – COMPUTER ARCHITECTURE

(Common to Information Technology and B.E. (Part-Time) Third Semester Computer Science and Engineering)

(Regulation – 2004)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. Give an example each of zero-address, one-address, two-address, and three-address instructions.

2. Which data structures can be best supported using (a) indirect addressing mode (b) indexed addressing mode?

3. What is the purpose of guard bits used in floating point operations?

4. Give the booth's recoding and bit-pair recoding of the number 1000111101000101.

5. Why is the Wait-For-Memory-Function-Completed step needed when reading from or writing to the main memory?

6. How do control instructions like branch, cause problems in a pipelined processor?

7. What is the function of a TLB (translation look-aside buffer)?

8. An eight-way set-associative cache consists of a total of 256 blocks. The main memory, contains 8192 blocks, each consisting of 128 words.

   (a) How many bits are there in the main memory address?

   (b) How many bits are there in the TAG, SET and WORD fields?

9. Why are interrupt masks provided in any processor?

10. How does bus arbitration typically work?

PART B — (5 × 16 = 80 marks)

11. (i) Explain in detail the different types of instructions that are supported in a typical processor. (10)

(ii) Registers R1 and R2 of a computer contain the decimal values 1200 and 2400 respectively. What is the effective address of the memory operand in each of the following instructions?

(1) Load 20(R1), R5

(2) Add -(R2), R5

(3) Move #3000, R5

(4) Sub (R1)+, R5 (6)

12. (a) (i) Explain in detail the principle of carry-look-ahead adder. Show how 16-bit CLAs can be constructed from 4-bit adders. (12)

(ii) Perform the division on the following 5-bit unsigned integer using non-restoring division: 10101 / 00101. (4)

Or

(b) (i) Explain the working of a floating point adder/subtractor. (12)

(ii) Multiply the following pair of signed 2's complement numbers using bit-pair recoding of the multipliers : A = 010111, B = 101100. (4)

13. (a) (i) Explain how pipelining helps to speed-up the processor. Discuss the hazards that have to be taken care of in a pipe-lined processor. (12)

(ii) Give the sequence of control signals to be generated to fetch an instruction from memory in a single-bus organization. (4)

Or

(b) Explain in detail the working of a micro-programmed control unit. (16)

14. (a) (i) Discuss the address translation mechanism and the different page replacement policies used in a virtual memory system. (10)

(ii) A byte-addressable computer has a small data cache capable of holding eight 32 bit words. Each cache block contains one 32-bit word. When a given program is executed, the processor reads data from the following sequence of hex addresses –

200, 204, 208, 20C, 2F4, 2F0, 200, 204, 218, 21C, 24C, 2F4. The pattern is repeated 4 times. Assuming that the cache is initially empty, show the contents of the cache at the end of each pass, and compute the hit rate for a direct mapped cache. (6)

Or

(i) Discuss the various mapping schemes used in cache design. Compare the schemes in terms of cost and performance. (10)

(ii) Consider a two-level cache with access times of 5 ns, and 80 ns respectively. If the hit rates are 95%, and 75% respectively in the two caches, and the memory access time is 250ns, what is the average access time? (6)

(a) (i) Explain the use of vectored interrupts in processors. Why is priority handling desired in interrupt controllers? How do the different priority schemes work? (10)

(ii) Discuss the data transfer mechanism of the PCI bus. (6)

Or

(b) (i) Explain how data may be transferred from a hard disk to memory using DMA including arbitration for the bus. Assume a synchronous bus, and draw a timing diagram showing the data transfer. (10)

(ii) Discuss the salient features of the USB operation. (6)
