J 1233

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2006.

Third Semester

Information Technology

IF 242 — DIGITAL SYSTEM DESIGN

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Convert $(10\,10\,11\,10\,10)_2$ to hexadecimal.

2. Convert $(2C9)_{16}$ to decimal.

3. Convert $(A + B)$ to min terms.

4. Give the logic symbols and truth tables for an XOR gate and XNOR gate.

5. Represent the half–adder and full–adder operations with the help of truth tables.

6. Why NAND and NOR gates are called universal gates?

7. What are clocked sequential circuits and specify the advantage of clocked sequential circuits.

8. What are the memory elements used in a clocked sequential circuit? Discuss any one memory element?

9. Given a transition table for an asynchronous network, how can you determine if any races are present?

10. State the primary objective in choosing a state assignment for

    (a) Synchronous networks

    (b) Asynchronous networks.

PART B — (5 × 16 = 80 marks)

11. Find a hazard–free realization for each of the following functions using o 3–input NOR gates.

(i) $F(a,b,c,d) = \Sigma m\,(0,2,6,7,8,10,13)$.

(ii) $F(a,b,c,d) = \Sigma m\,(2,3,6,7,8,10,13)$.

12. (a) (i) State duality principle. Give relevant examples.

(ii) Simplify the Boolean function $F(x,y,z) = \Sigma\,(0,2,4,5,6)$ usin K–map.

(iii) Simplify the Boolean function $F(x,y,z) = \Pi\,(0,2,5,7)$ usin K–map. (5

Or

(b) Simplify the following Boolean function by using Quine–Mc Cluskey method $F = \Sigma\,(0,1,2,8,10,11,14,15)$. Illustrate the simplification process step by step. (16)

13. (a) Using AND and OR gates, find a minimum network to realize $F(a,b,c,d) = M_1\,M_2\,M_5\,M_9\,M_{10}\,M_{14}$.

(i) Using two level logic. (8)

(ii) Using three level logic. (12 gates inputs minimum) (8)

Or

(b) An implication gate has two inputs (X and Y); the output is 1 except when $X = 1$ and $Y = 0$.

(i) Show that the implication gate by itself is functionally complete. (8)

(ii) Realize $F = A'B + AC'$ using only implication gates. (Only $A, B, C, 0$ and 1 may be used as gate inputs. Four gates are sufficient. (8)

(a) (i) Give the truth table, logic diagram for a full adder circuit and discuss the same. (8)

(ii) Distinguish between encoder and decoder circuits. Give examples for the same. (8)

Or

(b) (i) Implement the following function with a multiplexer $F(A, B, C, D) = \Sigma(0, 1, 3, 4, 8, 9, 15)$. (8)

(ii) A combinational circuit is defined by the functions :

$$F_1(A, B, C) = \Sigma(3, 5, 6, 7)$$
$$F_2(A, B, C) = \Sigma(0, 2, 4, 7)$$

Implement the circuit with a PLA having three inputs, four product terms and two outputs. (8)

5. (a) (i) Design an asynchronous BCD down counter using JK flip flops and verify its operation. (10)

(ii) What are edge triggered flip flops? Discuss. (6)

Or

(b) Design a count which counts in the following sequence :

0000, 1000, 1100, 1010, 1110,

0001, 1001, 1101, 1011, 1111, 0000 ...

(i) Use clocked T flip flops, AND gates and OR gates. (8)

(ii) Use clocked D flip flops and NOR gates. (8)