J 1236

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2006.

Third Semester

Information Technology

IF 245 — COMPUTER ARCHITECTURE

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Define MIPS rate and throughput rate.

2. How should an instruction format be designed?

3. What is data path?

4. What is the necessity of branching?

5. Define hit rate and miss penalty.

6. Mention the limitation of USB.

7. How throughput can be increased in parallel processing?

8. List the difference between scalar and vector processor.

9. Differentiate control driven organization and data driven organization.

10. Give the instruction format of the RISC machine.

PART B — (5 × 16 = 80 marks)

11. (i) Explain the process of instruction execution cycle when an interrupt occurs. (8)

(ii) How do you evaluate a given system? Explain various parameter of performance equation. (8)

12. (a) (i) Draw and explain the micro programmed control unit.

(ii) Explain the process of next address generation using M programmed control.

(iii) How data hazards can be prevented in the instruction pipelining

Or

(b) Explain Booth's algorithm and find the solution for the multiplication +14 with –5

Multiplicand → 01110 (+14)

Multiplier →11011 (–5).

13. (a) (i) Describe Virtual memory organization with necessary diagram.

(ii) Explain the features of SCSI bus.

Or

(b) (i) Explain the drawbacks in programmed I/O and interrup driven I/O.

(ii) Describe the different types of RAMs and their applications. (8)

14. (a) (i) Explain the various segments of instruction pipeline with neat diagram. (8)

(ii) Briefly explain how parallelism is achieved in uniprocessor system. (8)

Or

(b) (i) Explain in detail how floating point addition be performed in arithmetic pipeline with necessary diagram. (10)

(ii) Explain the function of a vector processor. (6)

5. (a) (i) Compare and contrast of RISC over CISC. (6)

(ii) Explain the functional unit of static data flow computer architecture with diagram. (10)

Or

(b) (i) Compare static dataflow computer and dynamic dataflow computer. (8)

(ii) Explain the architecture of a RISC processor with necessary diagram. (8)
