S 9098

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2006.

Third Semester

Computer Science and Engineering

CS 232 — DIGITAL SYSTEMS

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. Given $(327)_9 = (x)_5$. Solve for x.

2. Determine the Gray code for decimal 43.

3. Show that a positive logic AND gate is the same as a negative logic OR gate.

4. Implement an exclusive OR gate using a two input multiplexer.

5. Why is the ROM inadequate for VLSI circuits and systems?

6. What is a (p,n,m) PLA?

7. Describe the behaviour of a T flip-flop by means of a table.

8. What is the minimum number of flip-flops needed to build a counter of modulus 18?

9. What is a static 1 hazard?

10. When is a sequential machine said to be strongly connected?

PART B — ($5 \times 16 = 80$ marks)

11. (a) (i) What is a redundant prime implicant? (4)

(ii) Using a Karnaugh map, determine the MSP form of $\sum(1, 3, 5, 7, 9, 13, 15, 31) + \sum_{\phi}(27, 30)$. (12)

Or

(b) (i) Show that the $84\overline{2}\,\overline{1}$ code is self complementing. (8)

(ii) Show that the NAND connective is not associative. (8)

12. (a) (i) Implement the function $\sum(1, 2, 4, 5)$ using a 3 line to 8 line decoder. (6)

(ii) Explain how a 4 line to 16 line decoder can be built using 2 to 4 line decoders. (10)

Or

(b) (i) Draw neat sketches showing unprogrammed AND gate and unprogrammed OR gate in PLD (programmable logic devices) notation. (6)

(ii) Implement the functions $\sum(0, 1, 2, 5, 7)$ & $\sum(1, 2, 4, 6)$ using a 8×2 PROM. (10)

13. (a) (i) What is iterative design? Draw a neat sketch showing the basic iterative circuit model. (6)

(ii) Explain how you will build a 8 bit adder/subtractor using two 74 LS83s. (10)

Or

(b) (i) State the relative merits of PAL and PLA. (6)

(ii) Implement the Boolean expressions $F_1 = \bar{x}z + \bar{y}\,\bar{z}$ and $F_2 = \bar{x}y + \bar{x}z + x\bar{y}$ using a PLA. (10)

14. (a) (i) Explain the working of a master-slave SR flip-flop. (6)

(ii) Draw the logic diagram of a MOD-8 twisted ring counter and determine its counting sequence. (10)

Or

(b) (i) Draw and explain a logic diagram depicting two registers X and Y of three flip flops each so that Y can be transferred into X or the 1's complement of Y can be transferred into X. (8)

(ii) If a binary machine handles negative numbers in the true magnitude form, how would – 4 be stored in a register with a sign bit and 4 bits representing magnitude? How would – 4 be stored if the same machine stored numbers in the 1's complement system? Repeat for a 2's complement system. (8)

15. (a) (i) Distinguish between Mealy machines and Moore machines. (6)

(ii) What is an ASM chart? How is it derived? (10)

Or

(b) (i) State three simple guidelines for obtaining state assignments. (6)

(ii) Show that no static '1' hazard can occur in a two level OR-AND gate network realisation of a switching function. (10)

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