S 9102

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2006.

Fourth Semester

Computer Science and Engineering

CS 238 — COMPUTER ARCHITECTURE – I

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is meant by stored program concept? Discuss.

2. What are the factors to be considered while choosing the addressing modes for a processor?

3. Discuss the IEEE format for representing single precision floating-point numbers.

4. How is a carry-look-ahead faster than a ripple-carry adder?

5. What are the relative merits and demerits of hardwired control and micro-programmed control?

6. Compute the effective CPI for a processor, assuming the following instruction mix :

Instruction class	Clock cycle count	% age
ALU	1	40
Loads	4	15
Stores	3	10
Branches taken	3	20
Branches not taken	2	15

7. Give functional diagram of the basic cell of an associative memory unit and discuss.

8. What is an interleaved memory organization?

9. Discuss the typical sequence of operations that a processor does when it receives an interrupt call.

10. What is an I/O processor?

PART B — (5 × 16 = 80 marks)

11. (a) (i) Discuss the various addressing modes supported by various processors, bringing out their applicability. (12)

(ii) What are the issues to be considered while designing the instruction formats? (4)

Or

(b) (i) Register R5 is used in a program to point to the top of the stack. Write a sequence of instructions using the Index, Autoincrement and autodecrement addressing modes to perform the following, assuming that the word length is 32 bits and the memory is byte addressable :

(1) Pop the top two items off the stack, add them and then push the result onto the stack.

(2) Copy the fifth item from the top into register R3.

(3) Remove the top ten items from the stack. (12)

(ii) Write a program that can evaluate the expression A × B + C × D in a Single-accumulator processor. Assume that the processor has load, Store, Add and Multiply instructions and that all values fit in the accumulator. (4)

12. (a) (i) Discuss the non-restoring division algorithm and simulate the same for the unsigned numbers A = 10101 and B = 00101. (12)

(ii) Discuss the principle of operation of a Booth's multiplier. (4)

Or

(b) (i) Discuss the organization and functioning of a floating point adder/subtractor unit with a neat diagram. (12)

(ii) Consider a 12-bit, floating-point number with one sign bit, a 5-bit exponent and a 6-bit fractional normalized mantissa where the base is 2 and the exponent is represented in excess -15 format. Represent the numbers +1.7 and –0.012 in this format. (4)

13. (a) (i) Give the organization of a typical hardwired control unit and explain the functions performed by the various blocks. (8)

(ii) Write down the sequences of steps with respect to the single bus organization, in order to do the following operation :

ADD (R1), disp. (R2), where the format is ADD dst, src, and the instruction is one word only. (8)

Or

(b) (i) Distinguish between a pipelined and a non-pipelined instruction unit. (4)

(ii) Discuss the hazards that might arise in a pipelined unit and suggest ways of overcoming /minimizing them? (12)

14. (a) (i) Discuss the various mapping techniques used in cache memories. (12)

(ii) A computer system has a main memory consisting of 16 M words. It also has a 4K-word cache organized in the block-set-associative manner, with 4 blocks per set and 32 words per block. Calculate the number of bits in each of the TAG, SET and WORD fields of the main memory address format. (4)

Or

(b) (i) Explain the concept of virtual memory with any one virtual memory management technique. (12)

(ii) What is a TLB? How is it useful? (4)

15. (a) (i) What is meant by programmed data transfer? (4)

(ii) What is a DMA controller? How is it useful in a computer system? (12)

Or

(b) (i) Distinguish between serial and parallel interfaces. (4)

(ii) Discuss the storing, organization and accessing of data in an optical disk. (12)