**D 024**

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2003.

Third Semester

Computer Science and Engineering

CS 232 — DIGITAL SYSTEMS

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Find the hexadecimal equivalent of the octal number 153.4.

2. Show that the excess – 3 code is self–complementing.

3. State and prove Demorgan's theorem.

4. Show that a positive logic NAND gate is the same as a negative logic NOR gate.

5. Distinguish between a decoder and a demultiplexer.

6. Derive the characteristic equation of a JK flip–flop.

7. State the relative merits of series and parallel counters.

8. What are Mealy and Moore machines?

9. A shift register comprises of JK flip–flops. How will you complement the contents of the register?

10. What is a dynamic hazard?

11. (i) Explain how you will construct an $(n + 1)$ bit Gray code from an $n$ bit Gray code.

(ii) Determine the MSP form of the switching function $F = \Sigma$ (0, 1, 4, 5, 6, 11, 14, 15, 16, 17, 20–22, 30,32, 33, 36, 37, 48, 49 52, 53, 59, 63)

12. (a) Implement the switching function whose octal designation is 274 using NOR gates only.

Or

(b) Design a switching circuit that converts a 4 bit binary code into a 4 bit Gray code using ROM array.

13. (a) Implement a binary serial adder using an SRFF programmable logic array.

Or

(b) Using D flip–flops, design a synchronous counter which counts in the sequence.

000, 001, 010, 011, 100, 101, 110, 111, 000.

14. (a) (i) Convert the following mealy machine into a Moore machine :

| | *Ns*, *Z* $x_1\,x_2$ | | | |
|---|---|---|---|---|
| *PS* | 00 | 01 | 11 | 10 |
| *A* | *A*, 0 | *A*, 1 | *B*, 0 | *A*, 1 |
| *B* | *A*, 1 | *B*, 0 | *B*, 1 | *B*, 0 |

(ii) Minimise the following state table :

| | Ns, Z $x$ | |
|---|---|---|
| *PS* | 0 | 1 |
| *A* | *A*, 0 | *D*, 1 |
| *B* | *C*, 1 | *D*, 0 |
| *C* | *B*, 0 | *E*, 1 |
| *D* | *D*, 1 | *A*, 1 |
| *E* | *E*, 0 | *G*, 1 |
| *F* | *G*, 0 | *E*, 0 |
| *G* | *D*, 1 | *A*, 1 |
| *H* | *D*, 1 | *C*, 1 |

Use Paull and Unger's implication chart.

Or

(b) Using JK flip–flops, design a synchronous sequential circuit having one input and one output. The output of the circuit is a 1 whenever three consecutive 1's are observed. Otherwise the output is zero.

15. (a) Implement the switching function $F = \Sigma$ (0, 1, 3, 4, 8–12) by a static hazard free two level OR–AND gate network.

Or

(b) Show that no static 0 (static 1) hazard can happen in a two level AND–OR (OR–AND) realisation of a switching function F.

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