

**D 091**

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2003.

Third Semester

Information Technology

IF 245 — COMPUTER ARCHITECTURE

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Discuss the stored program concept. What are its advantages and disadvantages?
2. Define the terms software compatibility and hardware compatibility. What role have they played in the evolution of computers?
3. What are the requirements to be satisfied by an instruction set?
4. Discuss the relative merits and demerits of a hardwired control unit and a microprogrammed control unit.
5. What is a TLB? What is its use?
6. A two level memory ( $M_1$ ,  $M_2$ ) has the access times  $t_{A1} = 10^{-8}$  sec. and  $t_{A2} = 10^{-3}$  sec. What must the hit ratio  $H$  be in order for the access efficiency to be atleast 65% of its maximum possible value?
7. Discuss the Flynn's classification of computers.
8. Consider an unpipelined machine that has 10 ns. clock cycles and uses four cycles for ALU operations and branches and five cycles for memory operations. Assume that the relative frequencies of these operations are 40%, 20% and 40% respectively. Suppose that due to clock skew and set up, pipelining the machine adds 1 ns of overhead to the clock. Ignoring any latency impact much speed up in the instruction execution rate will we gain from a pipeline.
9. Distinguish between RISC and CISC machines.
10. What is meant by reliability? How is it defined for a series and parallel system?

PART B — (5 × 16 = 80 marks)

11. (i) What are the different hazards that might arise in a pipeline? How are they overcome? (3)
- (ii) Give the organization of a floating point adder/subtractor unit and explain its operation. (3)
12. (a) (i) What is a stack processor? Show the stack states during the execution of  $Z = w + (3 \times (x - y)) + 2(v \times u)$ . (6)
- (ii) Discuss the different addressing modes used typically in RISC processors. (5)
- (iii) What are the different types of instructions found in processors? Discuss. (5)

Or

- (b) (i) How should an instruction format be designed? Discuss the different types of instruction formats, bringing out their relative advantages and disadvantages. (6)
- (ii) How do you determine the instruction execution speed of a processor?

Identify and briefly describe three distinct ways in which parallelism can be introduced into the micro architecture of a computer in order to increase its overall instruction execution speed. (10)

13. (a) (i) Give the organization of a two's complement multiplier and discuss its operation. (8)
- (ii) Discuss the organization of a microprogrammed control unit. How are branches implemented here? (8)

Or

- (b) (i) Show how a 64 bit adder can be constructed using 4-bit adder modules and 4 bit carry look ahead generator modules. What is the delay in generating  $C_{64}$  and  $S_{63}$  here? (8)
- (ii) Discuss any one binary division algorithm and simulate the same for  $25 \div 15$ . (8)

14. (a) (i) How is parallelism achieved in uniprocessor machines? Discuss. (6)
- (ii) Discuss about an interrupt driven transfer and a DMA transfer clearly bringing out the advantages and disadvantages of each technique. (10)

Or

- (b) (i) What are associative memories? How are they constructed and used? (8)
- (ii) Consider the following page address trace generated by a two level cache main memory scheme that uses demand paging and has a cache capacity of four pages :

1 6 4 5 1 4 3 2 1 2 1 4 6 7 4.

Assuming the cache initially has pages 1, 2, 3 and 4, show the cache trace if LRU policy is used for replacement. Contrast this with FIFO replacement. (8)

15. (a) Discuss the architectural features of the SPARC processor.

Or

- (b) (i) What are the different ways in which redundancy can be made use of provide fault tolerance? (6)
- (ii) Discuss the design principles used in typical RISC processors. (10)