R 8211

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2006.

Sixth Semester

Computer Science and Engineering

CS 340 — COMPUTER ARCHITECTURE — II

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. State Amdahl's law.

2. What is meant by effective address?

3. What is the necessity of instruction level parallelism?

4. When can data Hazard be created?

5. List out the merits of VLIW.

6. Differentiate between hardware and software speculation mechanism.

7. What is the meaning of communication latency?

8. Compare among the local node, home node and remote node.

9. List out five ways of input output system design.

10. What do you mean by fixed field decoding?

PART B — (5 × 16 = 80 marks)

11. (a) (i) Derive and explain the CPU performance equation. (6)

(ii) Suppose we have made the following measurements :

Frequency of FP operation (other than FPSQR) = 25%

Average CPI of FP operation = 4.0

Average CPI of other instructions = 1.33

Frequency of FPSQR = 2%

CPI of FPSQR = 20.

Assume that the two design alternatives are to decrease the CPI of FPSQR to 2 or to decrease the average CPI of all FP operation to 2.5. Compare these two design alternatives using the CPU performance equation. (10)

Or

(b) (i) Describe the structure of the recent compiler with suitable example. (10)

(ii) How to implement an instruction in RISC processor? Explain. (6)

12. (a) (i) What is Pipelining? Describe the pipeline hazards with suitable example. (10)

(ii) How many branch selected entries are in a (2, 2) predictor that has a total of 8 K bits in the prediction buffer? (6)

Or

(b) (i) What is dynamic scheduling? Explain the dynamic scheduling with an example. (10)

(ii) Consider a loop branch whose behaviour is taken nine times in a row, then not taken once. What is the prediction accuracy for this branch, assuming the prediction bit for this branch remains in the prediction buffer? (6)

13. (a) (i) Discuss the basic VLIW approach with suitable example. (8)

(ii) Explain the Vector processor with suitable example. (8)

Or

(b) (i) Explain the Super scalar processor with reference to its applications. (8)

(ii) What are the compiler speculation capabilities? Discuss. (8)

14. (a) Describe the basic structure of a centralized shared memory multiprocessor. (16)

Or

(b) With neat block diagram explain the basic structure of distributed shared memory architecture. (16)

15. (a) (i) Derive and explain the average time waiting in the queue in terms of the average service time and server utilization. (10)

(ii) Describe the RISC processor with its applications. (6)

Or

(b) (i) Suppose an I/O system with a single disk gets on average 50 I/O requests per second. Assume the average time for a disk to service an I/O request is 10 ms. What is the utilization of the I/O system? What is the mean number of I/O requests in the queue? (10)

(ii) Write a short note on stack processors. (6)
