A 245

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2005.

Fifth Semester

Electronics and Communication Engineering

EC 336 — COMPUTER ARCHITECTURE

(Common to Bio--Medical Engineering)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. Write the instruction format for indirect addressing mode and register addressing mode.

2. Define CPU.

3. What is coprocessor?

4. Define pipeline processing.

5. What is hardwired control?

6. Define nano programming.

7. What is the advantage of cache memory?

8. Define associate memory.

9. What is meant by bus arbitration?

10. Define DMA.

PART B — (5 × 16 = 80 marks)

11. Describe the different instruction format and addressing modes with example.

12. (a) (i) Explain the booth's algorithm in detail.

(ii) Describe the carry look adder with neat diagram.

Or

(b) (i) What is the function of coprocessor? How coprocessor can be differentiated from main processor?

(ii) Discuss the pipeline processing in detail.

13. (a) Write short notes on :

(i) microprogrammed control.

(ii) superscale processing.

Or

(b) Describe the CPU control unit with timing control with neat diagram.

14. (a) With neat diagram explain the direct–mapped Cache and Associative–mapped Cache.

Or

(b) Describe the virtual–memory address translation technique.

15. (a) Describe the method of data transfer from output device through DMA to CPU.

Or

(b) With neat diagram explain the IOP organization.

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