B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2005.

Third Semester

Electronics and Communication Engineering

EC 1203 — ELECTRONIC CIRCUITS — I

(Regulation 2004)

Time : Three hours   Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Why do you fix the operating point in the middle of the dc load line?

2. Explain one application JFET used as variable resistor.

3. With small signal equivalent circuit derive the input impedance of CB amplifier.

4. Define CMRR.

5. What are causes for upper cut-off frequencies in BJT?

6. Define class C operation of power amplifier.

7. Determine the cut-off frequency due to the by pass capacitor in the figure shown.
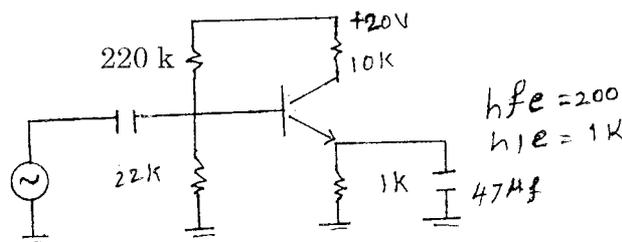
8. Why class A amplifier must not be operated under no signal conditions?

9. Derive the ripple factor of FWR.

10. What are the limitations of using Zener diode regulator?

11. (i) Draw a cascode amplifier and its equivalent circuit. What are the special features of cascode amplifier. (6)

    (ii) Derive the voltage gain, input impedance and out impedance of the above cascode amplifier. (10)

12. (a) (i) Locate the operating point of the circuit shown. (6)
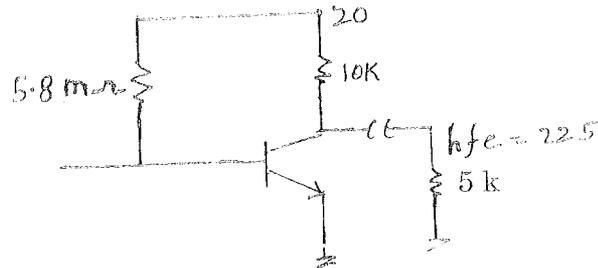
    (ii) Derive the stability factor $\dfrac{\delta I_C}{\delta h f_e}$ in a self bias circuit. What are the design considerations to make the stability factor independent of hf_e variation? (10)

Or

    (b) Explain the function of differential amplifier with neat circuit. Derive its Ad, Ac and CMRR. How CMRR can be improved?

13. (a) (i) What are the different biasing methods of JFET? (6)

        (ii) Why bootstrapping is done in a buffer amplifier? (6)

        (iii) Draw the characteristics of JFET and mark its regions of operation. (4)

Or

    (b) Determine the bandwidth of the amplifier shown.

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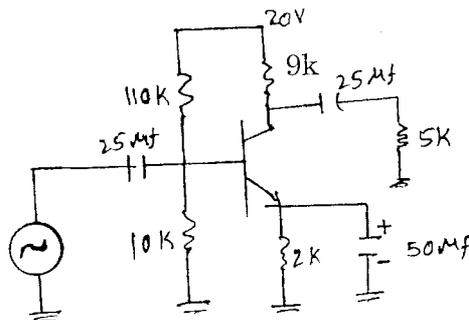
$rb'e = 1.1k$

$cb'e = 3 pf$

$cb'c = 100 pf$

$hfe = 225$.

14. (a) Explain class A power amplifier and derive its efficiency.

Or

(b) Explain class B power amplifier and derive its efficiency.

15. (a) Explain the working of FWR with π filter. Derive its ripple factor.

Or

(b) How regulation of output voltage is obtained against line and load variation in SMPS.