A 262

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2001.

Fifth Semester

Electrical and Electronics Engineering

EE 333 — DIGITAL SYSTEMS

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Convert the following numbers with the indicated bases to decimal $(4310)_5$ and $(198)_{12}$.

2. What bit must be complemented to change an ASCII letter from capital to lowercase and vice versa?

3. Simplify the following Boolean expressions to a minimum number of literals :

   (a) $(X+Y)(X+\overline{Y})$

   (b) $XY+\overline{X}Z+YZ$.

4. What are prime implicants?

5. What is noise margin?

6. What is fan–out of a gate?

7. What is meant by the term state–reduction?

8. How does the operation of an asynchronous input differ from that of a synchronous input?

9. Whether PAL is same as PLA? Explain.

10. Distinguish between decoder and demultiplexer.

PART B — (5 × 16 = 80 marks)

11. (i) Perform each of the following computations using signed, 8 bit words in 1's complement and 2's complement binary arithmetic : (10)

(1) $(+95)_{10} + (-63)_{10}$

(2) $(+42)_{10} + (-87)_{10}$

(3) $(-13)_{10} + (-59)_{10}$

(4) $(+38)_{10} + (-38)_{10}$

(5) $(-105)_{10} + (-120)_{10}$.

(ii) Design a parity circuit that will assign a parity bit to the 8421 BCD code in an odd parity system. (6)

12. (a) (i) Simplify the following Boolean function in (1) Sum of products and (2) Product of sums.

$F(A, B, C, D) = \Sigma (0, 1, 2, 5, 8, 9, 10)$ (10)

(ii) Plot the following Boolean function on a Karnaugh map and simplify it.

$F (w, x, y, z) = \Sigma (0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$. (6)

Or

(b) (i) Determine the prime implicants of the given function using Tabulation method.

$F(w, x, y, z) = \Sigma (1, 4, 6, 7, 8, 9, 10, 11, 15)$. (10)

(ii) Implement the following function with NAND gates

$F (x, y, z) = \Sigma (0, 6)$. (6)

13. (a) (i) Draw the circuit of TTL NAND gate and explain its operation. (8)

(ii) Draw the logic diagram of full subtractor and explain its operation. (8)

Or

(b) (i) Draw the circuit of NMOS NAND gate and explain its operation. (8)

(ii) Draw the logic diagram of a 4–bit binary adder/subtractor using full adder and explain. (8)

14. (a) (i) Realize D flip flop using NOR gates and explain its operation. (8)

(ii) Explain the operation of JK master slave flip flop with suitable diagrams. (8)

Or

(b) (i) Using ROM, design a combinational circuit which accepts 3 bit number and generates an output binary number equivalent to square of input number. (8)

(ii) Explain the operation of bipolar RAM cell with suitable diagrams. (8)

15. (a) (i) Design a 3 bit synchronous Gray code counter using T flip flop. (10)

(ii) A combinational circuit is defined by the functions

$F_1 (A, B, C) = \Sigma (3, 5, 6, 7)$

$F_2 (A, B, C) = \Sigma (0, 2, 4, 7)$

Implement the circuit with PLA. (6)

Or

(b) (i) Minimize the state table shown given below : (10)

	Next State, Z (output)	
Present State	X (Input)	
	0	1
A	A, 0	B, 0
B	C, 0	D, 0
C	A, 0	D, 0
D	E, 0	F, 1
E	A, 0	F, 1
F	G, 0	F, 1
G	A, 0	F, 1

(ii) Implement the following function with multiplexer :

$F (A, B, C, D) = \Sigma (0, 1, 3, 4, 8, 9, 15)$ (6)