B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2005.

Sixth Semester

Electrical and Electronics Engineering

EE 350 — COMPUTER ARCHITECTURE

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is an instruction cycle? Write the steps occurred in the execution of the instruction ADD A, B where A, B are memory locations.

2. What is zero-address instruction? Write the instructions for multiplying two numbers using zero-address instruction.

3. What is a serial adder? What are its components?

4. Write the sequence of events in Booth's algorithm for multiplying 7 by 3.

5. What are the adddress-sequencing capabilities required in a control memory?

6. What are the functions provided by the fields in a microinstruction format?

7. Define locality of reference. What are its types?

8. What are the different write policies followed in systems using cache memory?

9. What is the function of an I/O interface?

10. Write the sequence of events in destination-initiated transfer using handshaking.

PART B — (5 × 16 = 80 marks)

11. (i) Define addressing mode. What are the advantages of using addressing mode techniques? Classify addressing modes and explain each type with examples. (10)

    (ii) Describe the features of microcomputer. (6)

12. (a) (i) Draw the diagram of a carry-lookahead adder and explain the carry-lookahead principle. (8)

(ii) Draw the block diagram of a bit-sliced CPU and explain its working. (8)

Or

(b) (i) What are the problems associated with hardware implementation of division operation? Explain the different ways of implementing division operation in hardware. (10)

(ii) Write the steps involved in addition and subtraction of floating point numbers. What are the factors to be considered in performing floating-point arithmetic operations? (6)

13. (a) (i) Explain the working of a microprogram sequencer for a control memory. (8)

(ii) Classify microinstructions and explain their characteristics. (8)

Or

(b) (i) Explain the various design methods used in hardwired control. (8)

(ii) Explain the working of a nanoprogrammed computer. (8)

14. (a) (i) Explain the various mapping functions used for mapping main memory blocks into cache lines. (9)

(ii) Draw the block diagram of a associative memory and explain its working. (7)

Or

(b) (i) Explain the use of memory interleaving in high speed memories. (7)

(ii) Explain the design issues of virtual memory. (9)

15. (a) (i) With a help of a diagram, explain the DMA transfer in a microprocessor. (8)

(ii) With the help of a flow chart, explain the steps involved in CPU-IOP communication. (8)

Or

(b) (i) Explain the various ways of establishing the priority of simultaneous interrupts. (8)

(ii) Explain the different ways of transferring data serially between two units. (8)

_____

B 353