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B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2003.

Third Semester

Computer Science and Engineering

CS 232 – DIGITAL SYSTEMS

Time : Three hours   Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Find the decimal equivalent of $(346)_7$.

2. Find the complement of $x + yz$.

3. Write down the truth table of a half subtractor.

4. Distinguish between positive logic and negative logic.

5. How will you convert a JK flip–flop into a D flip–flop?

6. When is a counter said to suffer from lockout?

7. Distinguish between synchronous and asynchronous sequential logic circuits.

8. What is a shift register?

9. When is a sequential machine said to be strongly connected?

10. What is static 1 hazard?

PART B — (5 × 16 = 80 marks)

11. (i) State and prove DeMorgan's theorem.   (6)

    (ii) Determine the MSP (Minimum Sum of Product) form of
    $F(abcd) = \Sigma\,(0, 2, 4, 6, 8) + \Sigma_\varrho\,(10, 11, 12, 13, 14, 15)$.   (10)

12. (a) (i) Show that the NAND operation is not distributive over the AND operation. (8)

    (ii) Assuming that logic 1 is available, show that INHIBIT logic is functionally complete. (8)

Or

(b) Explain how will build a 16 input MUX using only 4 input MUXs.

13. (a) Using JK flip–flops, design a parallel counter which counts in the sequence.

000, 111, 101, 110, 001, 010, 000, ...

Or

(b) Draw and explain a block diagram of circuitry for two registers X and Y of three flip–flops each so that Y can be transferred into X or the 1's complement of Y can be transferred into X

14. (a) (i) Draw the state diagram of a JK flip–flop.

    (ii) Derive the state table of a serial binary adder. (6 + 10)

Or

(b) The state table of a machine is given below :

PS	NS, Z $x = 0$	NS, Z $x = 1$
A	A, 0	B, 0
B	C, 0	B, 0
C	D, 0	B, 0
D	A, 0	B, 1

By constructing an adjacency map of the states, determine a good state assignment.

15. (a) Write an explanatory note on derivation of ASM charts and realisation of ASM charts.

Or

(b) Show that dynamic hazards do not occur in two level AND–OR gate networks.

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