Register Number: ……..

M.E DEGREE EXAMINATIONS: MAY / JUNE 2013

Second Semester

APPLIED ELECTRONICS

ANE504 : Analysis and Design of Analog integrated Circuits

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 2 = 20 Marks)

1. Draw the small signal model of MOSFET.
2. Define weak inversion.
3. Define $S^{V_{ref}}_{V_{dd}}$ and TC(I_o) in voltage and current references.
4. Compare the use of emitter follower and push pull configuration as output stage
5. Draw the transfer characteristics of BJT and MOS Differential amplifier and compare
6. Define drift and state its effect on the performance of operational amplifiers
7. Differentiate between current sink and current source with schematic and characteristics
8. What are the advantages of cascode configuration?
9. What are the important performance parameters of VCO?
10. List the different sources of noises

PART B (5 x 16 = 80 Marks)

11. a) (i) Derive the complete small signal model for an NMOS transistor with $I_D = 100\ \mu A$, $V_{SB} = 1$ V, $V_{DS} = 2$ V, Device parameters are $\Phi_f = 0.3$ V, W = 10 μ m, L = 1 μ m, $\gamma = 0.5\ V^{0.5}$ $K' = 200\ \mu A / V^2$, $\lambda = 0.02\ V^{-1}$, $t_{ox} = 100$ angstroms, $\psi_o = 0.6$ V, $C_{Sbo} = C_{dbo} = 10$ f F. Overlap capacitance from gate to source and gate to drain is 1 f F Assume $C_{gb} = 5$ f F (8)

(ii) Draw and explain the high frequency model of BJT (8)

(OR)

b) (i) Obtain the expression for drain current of MOSFET in the Triode region and state its significance (7)

(ii) Define the various second order effects associated with MOSFET with relevant expression and also state the effect of these on MOS current (9)

12. a) (i) Explain the circuit of thermal voltage references and state need for startup circuits (6)

(ii) Draw the circuit of basic differential amplifier with active load and discuss the performance. What is the effect of mismatch of g_m on the CMRR of amplifier (10)

(OR)

b) (i) Analyse the pushpull output stage with necessary sketches (8)

(ii) Compare Emitter follower, source follower, pushpull output stages (8)

13. a) (i) Design a low drift op amp and explain (8)

(ii) Perform DC analysis of 741 operational amplifiers with schematic (8)

(OR)

b) (i) Discuss the effect of drain resistance mismatch and g_m mismatch on the performance of opamp, in particular on CMRR (10)

(ii) Compare the features of bipolar and MOS op amps (6)

14. a) (i) For a simple current mirror utilizing devices with threshold voltage as 0.5V, $k' = 387\mu A / V^2$, $V_A = 5V/\mu m$, $W/L = 3.6\ \mu m / .36\ \mu m$ and $I_{Ref} = 100\ \mu A$, find the minimum dc voltage required at the output and the output resistance. (8)

(ii) Explain the principle of Band Gap voltage reference with schematic (8)

(OR)

b) (i) Draw the circuit of a Wilson current mirror and derive expression for output resistance and minimum output voltage (6)

(ii) Explain the method of realizing telescopic OpAmps with schematic and compare with other realizations (10)

15. a) (i) Explain Application of Gilbert cell as four quadrant multiplier (6)

(ii) Discuss about the capturing process of PLL. Obtain expression for lock range and capture range (10)

(OR)

b) (i) Draw the MOSFET small signal model with various noise sources and explain. (10)

How does feedback improve noise performance?

(ii) Draw the noise model for various integrated circuit components (6)

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