M.E DEGREE EXAMINATIONS: JUNE 2013

Second Semester

APPLIED ELECTRONICS

ANE507**:** ASIC Design

Time: Three Hours   **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 2 = 20 Marks)

1.   Define the standard-cell based ASICs

2.   How to develop symbolic layout in library-cell design?

3.   Mention the advantage of metal metal antifuse

4.   How to program and erase the EEPROM transistor?

5.   Compare Xilinx LCA with Actel architecture

6.   Mention some of the errors, the netlist scanner can find.

7.   What are blocking and nonblocking assignments?

8.   Mention the rules to be followed in nine-valued system of VHDL synthesis

9.   How to measure reliability of any system?

10. Mention the significance of BIST.

PART B (5 x 16 = 80 Marks)

11. a) (i)   Describe the different types of masked gate array (MGA)   (10)

         (ii) Briefly explain transistor parasitic capacitance   (6)

(OR)

    b) (i)   Explain how to design a single-stage combinational CMOS logic cell   (6)

         (ii) Discuss in detail about logical effort   (10)

12. a) (i)   Describe the Altera MAX architecture   (8)

         (ii) Mention the purpose and procedure followed in Shannon's expansion theorem,   (8)
               with an example.

(OR)

    b) (i)   Analyze the DC characteristics of the Totem-pole output buffer   (6)

         (ii) Explain the Xilinx CLB, architechture.   (10)

13. a) (i)   How to find RC delay in Antifuse connections?   (6)

		(ii)	Explain the Xilinx FPGA design flow with relevant diagrams	(10)
			(OR)	
	b)	(i)	Explain the interconnect architecture of Altera MAX 5000	(8)
		(ii)	How to explore hierarchical design?	(8)

14.	a)	(i)	Describe the synthesis process of finite-state machine	(10)
		(ii)	Mention the types of simulators and their significance	(6)
			(OR)	
	b)	(i)	Explain performance driven synthesis with an example	(12)
		(ii)	Mention the significance of static timing analysis	(4)

15.	a)	(i)	Describe the concurrent fault simulation	(6)
		(ii)	Explain the built-in self test procedure	(10)
			(OR)	
	b)	(i)	Explain D-calculus with an example	(6)
		(ii)	Analyze the controllability and observability for all logic gates	(10)

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