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M.E DEGREE EXAMINATIONS: JUNE 2013

Second Semester

APPLIED ELECTRONICS

ANE510**:** Low Power VLSI Design

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 2 = 20 Marks)

1. Mention the sources of power dissipation in digital CMOS circuit.
2. What is meant by dynamic power dissipation?
3. How do glitches affect power dissipation?
4. Give the significance of the term power analysis.
5. What is meant by guarded evaluation?
6. Compare static and dynamic logic.
7. How is LNS applicable for low-power design?
8. List the sources of power dissipation in dynamic RAMs.
9. What is bus switching activity? Explain.
10. Mention the several contributors to CPU power dissipation that are influenced by software.

PART B (5 x 16 = 80 Marks)

11. a) (i) Derive an expression for the short circuit power dissipation in a CMOS inverter. Also discuss the methods adopted to minimize power dissipation. (12)

    (ii) Explain the effect of supply voltage and threshold voltage on CMOS power. (4)

(OR)

    b) (i) Using the mathematical charged model, obtain the expression for the threshold voltage V_T of MIS diode. (10)

    (ii) Explain the impact of transistor sizing and technology scaling on low power circuits (6)

12. a) (i) Explain gate level analysis to estimate power in CMOS circuit (8)

    (ii) Give the procedure for Monte Carlo power simulation. List the precautions to be taken in this method. (8)

(OR)

    b) (i) Derive an expression for conditional probability and frequency. (8)

(ii) What is entropy? How do you estimate power dissipation in the case of combinational logic circuit based on entropy analysis. (8)

13. a) (i) How is the reduction in switching activity achieved in combinational logic circuits? (8)

(ii) Show that SPL is a promising style for low power operation. (8)

(OR)

b) With neat diagrams explain the following low power full adder circuits (8)

(i) Complementary Pass-transistor Logic (CPL)

(ii) Static and dynamic Differential Cascode Voltage Switch Logic (DCVSL) (8)

14. a) Investigate the different low power techniques for SRAM.

(OR)

b) (i) Explain the method of obtaining low power in layout design for standard cell libraries. (8)

(ii) How does complementary adiabatic logic computation differ from static CMOS gate in power dissipation? (8)

15. a) (i) What is the principle of pre computation logic? Explain pre computation architecture based on Shanon's decomposition. (8)

(ii) Write a survey on the different hardware/software trade-offs that have come up for the power optimization of software. (8)

(OR)

b) (i) With a neat block diagram, explain the design flow at algorithmic level. Explain the DCM technique for realization of low power FIR filters. (10)

(ii) Explain the method of power optimization using operation reduction. (6)

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