Register Number:……..

B.E., DEGREE EXAMINATIONS MAY/JUNE 2013

Fourth Semester

ECE103: DIGITAL ELECTRONICS

(Common to EEE & EIE)

Time: Three Hours **Maximum Marks: 100**

Answer ALL Questions:-

PART A (10x1=10 Marks)

1. The minimum number of flip flops required for a mod-12 ripple counter is

   A. 6 B. 3 C. 12 D. 4.

2. Convert the decimal number $(187)_{10}$ to 8-bit binary

   A. $(101110112)_2$ B. $(110111012)_2$ C. $(101111012)_2$ D. $(101111002)_2$

3. How many inputs will a decimal-to-BCD encoder have?

   A. 4 B. 8 C. 10 D. 16

4. Which of the following is not a weighted value positional numbering system:

   A. hexadecimal B. binary-coded decimal

   C. binary D. octal

5. How is a J-K flip-flop made to toggle?

   A.J = 0, K = 0 B.J = 1, K = 0 C.J = 0, K = 1 D.J = 1, K = 1

6. The terminal count of a modulus-11 binary counter is _____.

   A.1010 B. 1000 C.1001 D. 1100

7. On the third clock pulse, a 4-bit Johnson sequence is Q0 = 1, Q1 = 1, Q2 = 1, and Q3 = 0. On the fourth clock pulse, the sequence is _____.

   A. Q0 = 1, Q1 = 1, Q2 = 1, Q3 = 1 B. Q0 = 1, Q1 = 1, Q2 = 0, Q3 = 0

   C. Q0 = 1, Q1 = 0, Q2 = 0, Q3 = 0 D. Q0 = 0, Q1 = 0, Q2 = 0, Q3 = 0

8. The bit sequence 0010 is serially entered (right-most bit first) into a 4-bit parallel out shift register that is initially clear. What are the Q outputs after two clock pulses?

   A. 0000 B. 0010 C.1000 D. 1111

9. The storage element for a static RAM is the _____.

   A. diode B. resistor C. capacitor D. flip-flop

10. _____ are used at the inputs of PAL/GAL devices in order to prevent input loading from a large number of AND gates.

    A. Simplified AND gates B.Fuses C.Buffers D. Latches

PART B (10x2=20Marks)

11. Prove that the logical sum of all min terms of a Boolean function of 2 variables is 1.
12. Implement the given function using only NAND gate F(x,y,z)= ∑m(0,6).
13. Differentiate Decoder from Demultiplexer.
14. Convert (367)10 to Excess-3 code.
15. What is the drawback of SR FF? How is this minimized?
16. Convert a D FF into a T FF.
17. What is the cause for essential Hazard?
18. Draw block diagram for Moore model.
19. What is meant by memory expansion? Mention its limit.
20. What is PAL? How does it differ from PLA?

PART C (5x14=70Marks)

21. a) Find a minimal SOP representation for
    f(A,B,C,D,E)=∑m(1,4,6,10,20,22,24,26)+d(0,11,16,27) Using K-map method. Draw the circuit of the minimal expression using only NAND.

(OR)

b) Simplify the following function using Quine Mc Cluskey method

F(ABCD)=∑(0,2,3,6,7,8,10,12,13)

22. a) (i) Realize F(w, x, y, z)= Σ (1,4,6,7,8,9,10,11,15) using 8 to 1 Mux. (7)
    (ii) Draw the logic diagram of a BCD adder and explain its operation. (7)

(OR)

b) Design a carry look ahead adder with necessary diagrams.

23. a) Using D flip –flop ,design a synchronous counter which counts in the sequence
    000,001, 010, 011, 100, 1001,110,111,000.

(OR)

b) Design a negative- edge triggered ‘T flipflop’.

24. a) What is meant by universal shift register ?Explain the principle of operation of 4-bit universal shift Register.

(OR)

b) Obtain the Primitive Flow table for an asynchronous circuit that has 2 i/ps X & Y and o/p Z.An o/p Z=1 is to occur only during the input state XY=01 and then if& only if the i/p state XY=01 is preceded by the input sequence XY=01,00,10,00,10,00.

25. a) Implement the following functions with PLA.

i. $F_1(A,B,C)=\sum(0,1,2,4)$

ii. $F_2(A,B,C)=\sum(0,5,6,7)$

iii. $F_3(A,B,C)=\sum(0,3,5,7)$

(OR)

b) (i) Draw a RAM cell and explain its working. (7)

(ii) Explain the read cycle and write cycle timing parameters with the help of timing diagrams. (7)

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