Register Number: ……..

B.E., DEGREE EXAMINATIONS: MAY/JUNE 2013

Sixth Semester

ELECTRICAL AND ELECTRONICS ENGINEERING

ECE119: VLSI Design

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. The most important advantage of CMOS over BJT is
   a) Higher power dissipation
   b) Higher source capability
   c) Better noise margin
   d) Lower packing density
2. BiCMOS is a combination of
   a) pMOS and nMOS
   b) CMOS and ECL
   c) CMOS and IIL
   d) CMOS and BJT
3. A MOS technology is defined as 2λ. The equivalent dimension is
   a) 1 nm
   b) 0.1 nm
   c) 10 nm
   d) 2 nm
4. The important layers in MOS fabrication are
   a) Diffusion and oxide
   b) Diffusion, oxide and passivation.
   c) Oxide, polysilicon and metal
   d) Oxide, diffusion and metal
5. A pass transistor is usually constructed using one of the following -
   a) CMOS
   b) pMOS
   c) BJT
   d) CMOS and resistor
6. In pseudo nMOS circuit, the load is usually
   a) Discrete resistor
   b) pMOS enhancement mode device
   c) nMOS depletion mode device
   d) Open circuit
7. In a PLA device,
   a) Only AND array is programmable
   b) Only OR array is programmable
   c) Both AND and OR arrays are programmable.
   d) AND array is programmable but OR is fixed.
8. The programming technology used in XC4000 is
   a) Anti-fuse
   b) Fuse
   c) EEPROM
   d) SRAM

9. The *always* statement in Verilog HDL models

a) Combinational logic b) Concurrency

c) Sequential logic d) Memory

10. One of the following Company is a leading vendor of VLSI back-end tools -

a) Xilinx b) Cadence

c) Altera d) Microsoft

PART B (10 x 2 = 20 Marks)

11. Draw the symbols of pMOS and nMOS switches.
12. List any two processes that are used for CMOS fabrication.
13. What is a stick diagram? Where is it used?
14. State the minimum distance rules for layout.
15. Construct a 2-input NAND gate using CMOS.
16. What are the properties of CMOS domino logic device?
17. Define FSM.
18. What are the important steps in FPGA design flow? List any four.
19. What is behavior model?
20. Why is backend tool important?

PART C (5 x 14 = 70 Marks)

21. a) (i) Describe the twin-tub CMOS fabrication process. Use neat schematics. (10)

(ii) What is latch-up in CMOS? Explain with a diagram. (4)

(OR)

b) (i) What are the different processes that are used in MOS fabrication? Describe the importance of each. (10)

(ii) Compare CMOS and BJT technologies. (4)

22. a) From first principles, obtain the ratio of pull-up to pull-down impedance ratio for an nMOS transistor driven by another nMOS transistor.

(OR)

b) Describe a simple scaling model for nMOS transistor. Also, illustrate effect on various device parameters due to scaling.

23. a) A parity generator is to indicate parity of a binary number or word. Design the required circuit with sub-system design approach. Also, draw the stick diagram of the final circuit.

(OR)

b) (i) Draw the stick layout of switch level (nMOS) implementation of a 4:1 multiplexor. (10)

(ii) Explain how a 4:1 mux could be used to realize any *four* simple logic functions. Illustrate with a truth-table. (4)

24. a) Describe the architecture of PLA. Also, illustrate how the same could be used to implement combinational logic with an example.

(OR)

b) Describe the architecture of XC4000 FPGA with a neat schematic.

25. a) Verilog is a powerful simulation language. Using simple Verilog statements and syntax, illustrate how the same could be used to model combinational logic.

(OR)

b) (i) Describe the various HDL models used to describe hardware. Use Verilog statements and syntax to explain. (10)

(ii) Write short notes on back-end tools. (4)

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