Register Number: ……..

B.E DEGREE EXAMINATIONS: JUNE/JULY 2013

Seventh Semester

ELECTRONICS AND INSTRUMENTATION ENGINEERING

EIE117**:** VLSI Design

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. In MOS Fabrication, Etching techniques is used to remove
   a) Boron b) Phosphorus
   c) SiO2 d) Aluminium
2. Bi-CMOS technology is most widely used for implementing
   a) Only logic circuits b) Both I/O and driver circuits
   c) Only high speed parts of the system d) Only driver circuit
3. Increasing the width of the MOS transistor's to increase its transconductance will also increases
   a) input capacitance and area occupied b) Output capacitance
   c) Area occupied alone d) Input capacitance alone
4. In case of NMOS design, n-diffusion is represented in stick diagram in
   a) Red colour b) Blue colour
   c) Black colour d) Green colour
5. The actual logic function in Dynamic-CMOS logic is implemented by using
   a) NMOS Logic b) PMOS Logic
   c) CMOS Logic d) Bi-CMOS Logic
6. Multiplexers is also known as
   a) Data transmitter b) Data receiver
   c) Data selector d) channel
7. Once a PAL has been programmed
   a) it cannot be reprogrammed b) its outputs are only active HIGHs
   c) its outputs are only active LOWs d) Its logic capacity is lost
8. Type of memory used in FPGA is
   a) Dynamic RAM b) EE PROM
   c) Static RAM d) Flash memory
9. Which style of modelling has the lowest level of abstraction in VHDL
   a) Behavioural b) Data flow

c) Structural d) Mixed

10. Comments in VHDL are specified by _____dashed lines

a) two b) one

c) Three d) four

PART B (10 x 2 = 20 Marks)

11. Why polysilicon is used as gate electrode?
12. Define latch up problem
13. What is pull-up and pull-down transistor?
14. What is need of buffers?
15. Write the difference between dynamic CMOS logic and Clocked CMOS logic?
16. Draw the CMOS logic diagram for 2-input NAND gate
17. What are the logic gates that present in the basic programmable logic array (PLA) ?
18. List the elements inside the configurable logic blocks in FPGA.
19. Write the VHDL coding for half adder
20. What is a Process statement in VHDL?

PART C (5 x 14 = 70 Marks)

21. a) Explain in detail the enhancement and depletion mode transistor action with necessary diagram

(OR)

b) (i) Derive an current equation for NMOS transistor (7)

(ii) Write short notes on channel length modulation and body effect (7)

22. a) (i) Determine the pull-up to pull-down ratio for NMOS inverter driven by another inverter (7)

(ii) Determine the pull-up to pull-down ratio for NMOS inverter driven thrpugh one or more pass transistor (7)

(OR)

b) (i) Draw the stick diagram for two-input NOR gate in CMOS logic using suitable colour code (7)

(ii) Draw the circuit diagram for two-input NAND gate using Bi-CMOS Logic and explain its working (7)

23. a) (i) Explain the concept of two-phase clocking and also explain how to generate the two-phase clocking using D-flipflop (7)

(ii) Draw the circuit diagram for three input NAND gate using Dynamic CMOS logic and expain its working (7)

(OR)

b) Design 4x4 barrel shifter and explain its working

24. a) Discuss in detail about PLA and implement any Boolean function using PLA

(OR)

b) With neat diagram, explain in detail the internal architecture of FPGA

25. a) (i) Write VHDL code for D-flip flop and also the test bench for the same (7)

(ii) Write VHDL code for 3-bit up counter and also the test bench for the same (7)

(OR)

b) Write the VHDL code for 4:1 Multiplexer and 1:4 de-multiplexer and also the test bench

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