

M.E DEGREE EXAMINATIONS: JUNE 2013

Second Semester

EMBEDDED SYSTEMS

EST508: VLSI Architecture and Design Methodology

Time: Three Hours

Maximum Marks: 100

Answer all the Questions:-

PART A (10 x 2 = 20 Marks)

1. State Reed –Muller Expansion?
2. Define Consensus Theorem?
3. Define Neural Network?
4. Mention Analog Design Flow?
5. Draw ACTEL Act 1 logic module diagram?
6. What is programming technology, size of programming element, process, programming method in ALTERA FLEX?
7. Define EDIF? Purpose of it?
8. Write a CUPL program for BayBridgeTollPlaza?
9. Mention controllability and observability measures in automatic test pattern generation?
10. Mention VHDL Type Declarations?

PART B (5 x 16 = 80 Marks)

11. a) Design a binary toggle circuit that changes state with each rising edge of the clock input?
(Mention primitive state diagram, primitive state table, state map, excitation map and Y map, circuit diagram, a sequential timing diagram which generate a static hazard)

(OR)

- b) (i) VLSI design Methodologies in detail? (12)
(ii) State Shannon's expansion Theorem? (4)

12. a) Explain in detail about SWITCHED CAPACITOR FILTERS?

(OR)

- b) Explain in detail about SUBMICRON CMOS TECHNOLOGY?

13. a) (i) Define ACTEL ANTI FUSE in detail? (4)
(ii) Define Static RAM? (2)
(iii) Explain ALTERA FLEX in detail? (10)

(OR)

- b) (i) Mention clearly about Xilinx I/O blocks? (8)
(ii) Explain Clock and Power inputs? (8)

14. a) Explain in detail ALTERA MAX 9000 Architecture?

(OR)

- b) (i) Explain Xilinx XC3000 CLB Structure? (8)
(ii) Mention all low level design languages with each example? (8)

15. a) Explain Types of Simulation in detail?

(OR)

- b) Detail Explanation of FAULT SIMULATION?
