Register Number: ……..

M.E DEGREE EXAMINATIONS: APRIL/MAY 2014

(Regulation 2009)

Second Semester

APPLIED ELECTRONICS

ANE505: Computer Architecture and Parallel Processing

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 2 = 20 Marks)

1. What are the Flynn's classifications of computer architectures?
2. Mention any four application areas of parallel processing
3. When does aliasing problem occur in cache? How can it be overcome?
4. State and draw the two virtual memory models?
5. Compare CPA and CSA.
6. What is a backplane bus? Mention the various standards of it.
7. State the two lemmas used for converting program graph into an equivalent graph?
8. Differentiate static and dynamic dataflow
9. Give examples for parallel languages
10. What are the limitations of conventional UNIX?

PART B (5 x 16 = 80 Marks)

11. a) (i) Explain the different models of shared memory multiprocessors. (8)

(ii) Draw and explain the PRAM model of a multiprocessor and also discuss the various PRAM variants. (8)

(OR)

b) (i) Explain the various dependencies to be resolved while exploiting parallelism in detail. (8)

(ii) With neat diagrams, explain any one speedup performance laws. (8)

12. a) (i) Describe in detail about memory hierarchy technology (8)

(ii) Explain the various properties that must be satisfied by the data stored in memory (8)

(OR)

b) (i) Enumerate the various page replacement policies. (8)

(ii) What are the various types of memory interleaving? Explain. (8)

13. a) (i) Explain the two models of linear pipeline processor.Also discuss its performance (8)

(ii) Discuss the various mechanisms used for implementing instruction pipelining. (8)

(OR)

b) (i) Write about the design issues of super scalar and super pipeline processors. (8)

(ii) Explain the various message passing mechanisms in parallel architecture (8)

14. a) (i) What are the different types of Instructions? Explain each with one example. (8)

(ii) Explain the various vector-memory access schemes for the vector super computers (8)

(OR)

b) (i) Explain in detail about the concept of compound vector processing. (8)

(ii) Discuss about various context-switching policies and processor efficiencies (8)

15. a) Explain the various parallel models designed for Parallel programming

(OR)

b) Explain the OSF/1 architecture and its programming environment with focus on multithreading

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