

B.E DEGREE EXAMINATIONS: APRIL/MAY2014

(Regulation 2009)

Seventh Semester

ELECTRONICS AND COMMUNICATION ENGINEERING

ECE119: VLSI Design

Time: Three Hours

Maximum Marks: 100

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. The threshold voltage for the nMOS depletion mode device is
 - a) greater than V_{T0}
 - b) V_{T0}
 - c) Less than V_{T0}
 - d) None of the above.
2. Growth of thin layer of Silicon with controlled amount of impurities over the substrate is known as
 - a) Photolithography
 - b) Epitaxy
 - c) Diffusion
 - d) EBL
3. When a MOS device is in saturation, the effective channel length ----- when V_{ds} increases
 - a) Decreases
 - b) Does not vary
 - c) Increases
 - d) Varies randomly
4. The figure of merit of a MOS transistor is
 - a) $\frac{\mu}{L^2} \frac{1}{(V_{gs} - V_t)}$
 - b) $\frac{\mu}{L^2} (V_{gs})$
 - c) $\frac{\mu}{L^2} (V_{gs} - V_t)$
 - d) $\frac{\mu}{L^2} (V_t)$
5. Switches formed using transmission gate comprises of
 - a) Simple n-pass transistor
 - b) n-pass and p-pass in parallel
 - c) Simple p-pass transistor
 - d) n-pass and p-pass in serial
6. Charging and discharging of load capacitor leads to ----- power dissipation.
 - a) High
 - b) Low
 - c) Static
 - d) Dynamic
7. In FPGA ----- block provides the connection of internal CLB's with external packaged pins.
 - a) Input
 - b) Output
 - c) I/O
 - d) CLB
8. Which type of PLD should be used to program basic logic functions?
 - a) PLA
 - b) PAL

- c) CPLD
- d) FPGA
9. @ (clock) a = b; is
 - a) Delay-based timing control statement
 - b) Level-Sensitive timing control statement
 - c) Event-based timing control statement
 - d) Macro statement
10. Which of the following is used for verilog-based synthesis tools?
 - a) Intra-statement delay statements can be synthesized, but inter-statement delays cannot
 - b) Inter-statement delay statements can be synthesized, but intra-statement delays cannot
 - c) Initial values on the wires are always ignored
 - d) Synthesized results are identical for 'if' and 'case' statements.

PART B (10 x 2 = 20 Marks)

11. List the steps used in the n-well BICMOS Fabrication process.
12. Compare NMOS and PMOS devices.
13. What is Latch-up? How can it be prevented?
14. Mention the limitation of scaling of MOS devices.
15. Explain the principle of transmission gates.
16. Give the advantage of using Pass transistor logic.
17. Draw the FPG design flow.
18. What are the features of Altera Cyclone III device?
19. What is meant by continuous assignment statement in verilog HDL?
20. Compare blocking and non-blocking assignment in verilog.

PART C (5 x 14 = 70 Marks)

21. a) (i) With necessary diagrams explain the fabrication process of NMOS transistor. (8)
 (ii) Compare CMOS and BICMOS technologies. (6)
 (OR)
 b) (i) Discuss clearly the steps employed in SOI fabrication process with necessary diagrams. (10)
 (ii) Describe the depletion mode transistor action. (4)
22. a) (i) Write a note on scaling of MOS transistors. (7)
 (ii) With neat diagram, explain lambda-based design rules for contact cuts and vias. (7)
 (OR)
 b) (i) Draw and explain the characteristics of CMOS Inverter (8)
 (ii) Draw the layout of a CMOS inverter (6)

23. a) (i) Show that the pseudo-nMOS logic determines the required ratio of $\frac{Z_{p.u.}}{Z_{p.d.}} = \frac{3}{1}$ (8)
- (ii) Explain the C²MOS logic with an example. (6)
- (OR)**
- b) (i) Compare static and dynamic CMOS logic Circuits. (7)
- (ii) Implement the following function using CMOS gates (7)
- $$f(A, B, C) = \overline{A}BC + A\overline{B}C + ABC\overline{C}$$
24. a) (i) Enumerate salient features of Xilinx XC4000. (5)
- (ii) Draw and explain the Xilinx FPGA architecture. (9)
- (OR)**
- b) (i) Explain the finite state machine design using PLA. (7)
- (ii) Write a note on Altera Cyclone III Processor. (7)
25. a) (i) Illustrate with example, the branching statements in verilog. (6)
- (ii) Write a verilog program for 3 to 8 decoder in gate level description (8)
- (OR)**
- b) (i) Explain various delay modellciys used in verilog with an example. (6)
- (ii) Give a verilog structural gate level description of a 3-bit comparator. (8)
