Register Number: ……..

B.E DEGREE EXAMINATIONS: APRIL / MAY 2014

(Regulation 2009)

Sixth Semester

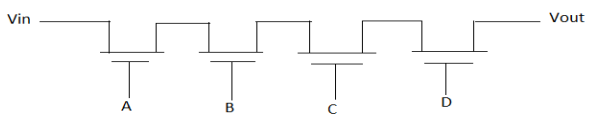
ELECTRICAL AND ELECTRONICS ENGINEERING

ECE119: VLSI Design

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions

PART A (10 x 1 = 10 Marks)

1. Arranging atoms in a single crystal fashion upon a single crystal substrate is called
   a) Etching b) Photolithography
   c) Epitaxy d) Masking
2. Which material is used as an insulator in SOI process
   a) Ceramic b) Graphite
   c) Carbon d) Sapphire
3. The threshold voltage of a P channel MOSFET is _____
   a) Zero b) Positive
   c) Negative d) Both a & c
4. Gate area (A_g) of a transistor is scaled by
   a) $1/\alpha^2$ b) $1/\alpha$
   c) $1/\beta$ d) $1/\beta^2$
5. 

   In the above diagram if A=B=C=D=1 the V_{out} = _____.
   a) V_{in} b) 1
   c) 0 d) A+B+C+D
6. Pseudo NMOS logic provides the following advantage
   a) Faster than other logics b) Less static power dissipation
   c) Immune to noise d) Requires less number of transistors
7. Which of the following PLD has programmable AND array and programmable OR array.
   a) FPGA b) ASIC
   c) PLA d) PAL
8. In FPGA which block provides connection of CLB's with external package pins
   a) Input b) Output
   c) IOB d) MUX
9. Connections between the hardware elements of a logic circuit can be declared with the keyword
   a) Cable b) Wire
   c) Connection d) Register
10. List the relational operators used in verilog HDL
    a) <, >, <=, >= b) +, -, /
    c) ~, l, ~□, & d) ==, ===, =

PART B (10 x 2 = 20 Marks)

11. List the various steps involved in the fabrication of integrated circuits.
12. What are the advantages of CMOS technology?
13. Define body effect.
14. What is the significance of stick diagram? Draw the stick diagram of NMOS and PMOS transistors.
15. Compare pass transistor and transmission gate.
16. Implement four way multiplexer using NMOS switch.
17. Categorize the programmable logic devices.
18. What are the internal blocks of an FPGA?
19. List the different types of modeling used in verilog.
20. Write a verilog code for a two bit comparator.

PART C (5 x 14 = 70 Marks)

21. a) Explain the fabrication of NMOS with neat diagrams.

    (OR)

    b) Describe the fabrication of CMOS using SOI process and enumerate the merits and demerits of SOI process.

22. a) Derive the drain to source current of N-Channel MOSFET in saturation and non saturation regions and draw the characteristics of Enhancement mode device.

    (OR)

    b) (i) What are the lambda based design rules? Explain. (6)

    (ii) Draw the circuit diagram and layout of two input CMOS NAND gate. (8)

23. a) (i) Explain dynamic CMOS logic for a three input NAND gate. (7)

(ii) With two input NOR gate describe the clocked CMOS logic. (7)

(OR)

b) (i) Illustrate the structured design of parity generator. (7)

(ii) Realize a 4 bit dynamic shift register using CMOS. (7)

24. a) Design and realize the following function using PLA

$$Y_1 = A\overline{B} + AC + D$$

$$Y_2 = \overline{A}B + B\overline{C} + \overline{D}$$

(OR)

b) (i) Explain the architecture and features of Xilinx XC4000. (10)

(ii) List the important features of Altera cyclone processor. (4)

25. a) Illustrate the different loops used in the behavioral modeling and give examples.

(OR)

b) (i) Explain the various data types used in verilog HDL. (7)

(ii) Write a verilog code for a negative edge triggered D flip flop. (7)

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