Register Number: ……..

B.E DEGREE EXAMINATIONS: APRIL/MAY 2014

(Regulation 2009)

Seventh Semester

ELECTRONICS AND INSTRUMENTATION ENGINEERING

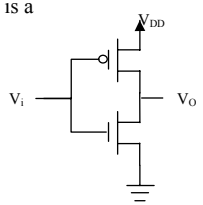
EIE117: VLSI Design

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

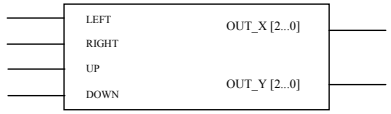
1. Which of the following is true for an NMOS transistor operating in its linear or triode mode? (Vgs =gate to source voltage, Vds = drain to source voltage, Vt = threshold voltage)
   a) Vds < (Vgs - Vt) b) Vds > (Vgs - Vt)
   c) Vgs < Vt d) Vgs = 0 V
2. Which of the following processing techniques would be used to create the source and drain regions of a transistor?
   a) Oxidation b) Ion implantation
   c) Sputtering d) Polysilicon deposition
3. A pseudo NMOS inverter produces _____ output.
   a) AC b) DC
   c) Pulse d) Zero
4. The given circuit diagram is a



   a) NMOS Inverter b) CMOS Inverter
   c) CMOS Gate d) NMOS Gate
5. A tally circuit's output depends on the _____
   a) Number of high inputs b) Number of low inputs
   c) Number of undefined state inputs d) All of the above
6. Clock tree doesn't contain following cell ___.
   a) Clock buffer b) AOI cell
   c) Clock Inverter d) None of the above
7. Once a PAL has been programmed:
   a) it cannot be reprogrammed. b) its outputs are only active LOWs
   c) its outputs are only active HIGHs d) its logic capacity is lost
8. What does a dot mean when placed on a PLD circuit diagram?
   a) A point that is programmable b) A point that cannot change
   c) An intersection of logic blocks d) An input or output point
9. Behavioural modelling is a..... style of modelling in VHDL.
   a) Concurrent b) Sequential
   c) Default d) Data Flow
10. NEXT statement is a/an ..... statement.
    a) conditional jump b) unconditional jump
    c) termination d) no operation

PART B (10 x 2 = 20 Marks)

11. Why is NAND gate preferred over NOR gate for fabrication?
12. Why SOI process is preferred over other fabricating technologies?
13. Give the expression for pull-up to pull-down ratio (*Zpu/Zpd*) for an NMOS inverter driven by another NMOS inverter.
14. What is the basic difference between a NMOS superbuffer and CMOS superbuffer?
15. Give the schematic of a XOR structure and brief on the same.
16. Draw a layout diagram for 3*3 barrel shifter.
17. What are Programmable Interconnects?
18. What is a FSM?
19. List all the operators available in VHDL programming.
20. Write the entity section of a VHDL program to implement the following block:



The 'left', 'right', 'up' and 'down' signals contain single bit values, and the 'out_x' and 'out_y' signals each contain 3 bits.

PART C (5 x 14 = 70 Marks)

21. a) i) What is body effect? Write the mathematical expression? (4)
    ii) Explain the different steps involved in n-well CMOS fabrication process with neat diagram. (10)

(OR)

	b)	i)	Plot the current-voltage characteristics of a NMOS transistor.	(4)
		ii)	List and discuss the various secondary effects of a MOS transistor.	(10)
22.	a)	i)	Draw a CMOS Inverter. Explain its transfer characteristics	(7)
		ii)	Draw a NOR-NOR implementation stick diagram for a 2-line to 4-line decoder.	(7)

(OR)

	b)	i)	What are the different color codes used for single poly silicon NMOS technology?	(4)
		ii)	Draw the CMOS diagram and stick diagram for a 2 input NAND and 2 input EX-OR gate	(10)
23.	a)		List the steps for combinational circuit design. Design a combinational circuit for a 8:1 multiplexer using NOR-NOR logic.	

(OR)

	b)		With a neat sketch explain the operation of dynamic CMOS clocking circuit and list some of its applications?	
24.	a)	i)	Give the classification of PLDs.	(4)
		ii)	Design a BCD to Excess-3 code converter and implement using a PLA	(10)

(OR)

	b)	i)	With a neat diagram discuss the structure of a FPGA.	(10)
		ii)	Implement the following two Boolean functions using a PROM. $F1(A,B,C)= \sum(0,1,2,4)$; $F2(A,B,C)= \sum (0,5,6,7)$	(4)
25.	a)	i)	What is the difference between function and procedure in VHDL?	(4)
		ii)	Give the truth table and write a VHDL program for a JK flipflop using behavioral modeling.	(10)

(OR)

	b)	i)	What is the difference between variable and signal? Also mention where each can be used appropriately.	(4)
		ii)	Give the truth table and write a VHDL program for a 8:1 MUX using all 3 types of modeling.	(10)

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