Register Number: …………………..

B.E DEGREE EXAMINATIONS: MAY/JUNE 2014

(Regulation 2013)

Second Semester

COMPUTER SCIENCE AND ENGINEERING

U13CST201: Digital System and Design

Time: Three Hours   **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. Convert $(634)_8$ to binary

   a) $(110)_2$ b) $(100)_2$

   c) $(110\ 011\ 100)_2$ d) $(110\ 011\ 101)_2$

2. The complement of (x+yz) is ……………..

3. How many 3-line-to-8-line decoders are required for a 1-of-32 decoder?

   a) 1   b) 2

   c) 4   d) 8

4. From the truth table of a half adder, …………….. is sum of the logic equation.

5. The bit sequence 0010 is serially entered (right-most bit first) into a 4-bit parallel out shift register that is initially clear. What are the Q outputs after two clock pulses?

   a) 0000   b) 0010

   c) 1000   d) 1111

6. A decoder is a combinational circuit that converts binary information from 'n' input lines to a maximum of …………….. unique output lines.

7. A BCD counter is a

   a) binary counter   b) full-modulus counter

   c) decade counter   d) divide-by-10 counter

8. In a combinational circuit, if output goes momentarily 0 when it should remain a 1, the hazard is known as …………….. hazard

9. Each PAL gate product is applied to an OR gate and, if combinational logic is desired, the product is ORed and then

   a) the polarity fuse is restored   b) sent to an inverter for output

   c) sent immediately to an output pin   d) passed to the AND function for output

10. PALs tend to execute ……………..logic.

PART B (10 x 2 = 20 Marks)

(Not more than 40 words)

11. What is the different classification of binary codes?

12. State Demorgan's theorem.

13. Show that the NAND connection is not associative.

14. Why parity checker is needed?

15. What is race around condition?

16. Mention the applications of a shift register.

17. How synchronous counters differ from asynchronous counters?

18. Describe how to detect and eliminate hazards from an asynchronous network?

19. Give the classification of memory.

20. Compare static RAMs and dynamic RAMs.

PART C (5 x 14 = 70 Marks)

(Not more than 400 words)

Q.No. 21 is Compulsory

21.   Implement the switching network: for BCD to Excess 3 conversion using PLA.

22. a)   Simplify the following Boolean Function using the Tabulation Method
            $F(A,B,C,D) = \Sigma m(1,4,\ 6,7,8,9,10,11,15)$.

(OR)

    b) (i) Express the Boolean Function F = A + B'C in a sum of minterms.   (7)

       (ii) Express the Boolean Function F = xy +x'z in a product of maxterms. (7)

23. a) (i) Convert 3287.510009810 into octal   (4)

       (ii) Implement the following Boolean function using 8X1 MUX   (10)
            $F(A, B, C, D) = \Sigma m (0, 2, 6, 10, 11, 12, 13) + \Sigma d (3, 8, 14)$

(OR)

    b)   Design a 4 bit magnitude comparator to compare two 4 bit number.

24. a)   Explain the operation of JK and clocked JK flip-flops with suitable diagrams

(OR)

b)   Design moore machine is that any input sequence ending with 101 will produce output x=1. output 1 does not reset. Use D flipflop.

25. a) (i)   Draw the state diagram of 'T' FF.   (4)

       (ii)   Design and explain the working of a synchronous mod – 3 counter.   (10)

(OR)

b)   Using SR flip flops, design a parallel counter which counts in the sequence 000,111,101,110,001,010,000 ………….

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