KUMARAGURU
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Register Number: ……..

B.E/B.TECH DEGREE EXAMINATIONS: DEC 2014

(Regulation 2009)

Third Semester

CSE105: COMPUTER ARCHITECTURE

(Common to CSE/IT)

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. _____ bus structure is usually used to connect I/O devices

   a) Single bus b) Multiple bus

   c) Star bus d) Rambus

2. In case of, Zero-address instruction method the operands are stored in _____

   a) Registers b) Accumulators

   c) Push down stack d) Cache

3. When we perform subtraction on -7 and 1 the answer in 2′s compliment form is _____

   a) 1010 b) 1110

   c) 0110 d) 1000

4. The most efficient method followed by computers to multiply two unsigned numbers is _____

   a) Booth algorithm b) Bit pair recording of multipliers

   c) Restoring algorithm d) Non restoring algorithm

5. A sequence of control words corresponding to a control sequence is called _____

   a) Micro routine b) Micro function

   c) Micro procedure d) None of the above

6. To increase the speed of memory access in pipelining, we make use of _____.

   a) Special memory locations b) Special purpose registers

   c) Cache d) Buffers

7. MFC is used to

a) Issue a read signal
b) Signal to the device that the memory read operation is complete
c) Signal the processor the memory operation is complete
d) Assign a device to perform the read operation

8. While using the direct mapping technique, in a 16 bit system the higher order 5 bits is used for _____.

a) Tag
b) Block
c) Word
d) Id

9. The time between the receival of an interrupt and its service is _____

a) Interrupt delay
b) Interrupt latency
c) Cycle time
d) Switching time

10. IDE disk is connected to the PCI BUS using _____ interface.

a) ISA
b) ISO
c) ANSI
d) IEEE

PART B (10 x 2 = 20 Marks)

11. Give the basic performance equation.
12. What is indirect addressing mode and indexed addressing mode?
13. What are the features of the hardwired control?
14. What do you mean by delayed branching?
15. What are the major characteristics of a pipeline?
16. What are superscalar processors?
17. Explain virtual memory.
18. What is RAID?
19. Explain Direct Memory Access.
20. What are vectored interrupts?

PART C (5 x 14 = 70 Marks)

21. a) Explain the various addressing modes.

(OR)

b) Explain in detail the data transfer between the memory & I/O unit.

22. a) Explain the organization of a Hardwired control unit. Mention its advantages and disadvantages.

(OR)

b) Explain the multiple bus organization structure with neat diagram.

23. a) Explain the various types of hazards in pipelining.

(OR)

b) Give the organization of the internal data path of a processor that supports a 4-stage pipeline for instructions and uses a 3-bus structure and discuss the same.

24. a) What are the various types of cache mapping mechanisms? Explain in detail.

(OR)

b) Discuss the virtual memory management technique in detail.

25. a) Describe the data transfer method using DMA.

(OR)

b) Explain in detail the various standard I/O interfaces.

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