KUMARAGURU
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Register Number: ……..

B.E / B.TECH DEGREE EXAMINATIONS: DEC 2014

(Regulation 2009)

Third Semester

ECE103: DIGITAL ELECTRONICS

(Common to CSE/ECE/MCT/IT)

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. Which of the following code is also known as reflected code?
   a) Excess-3 codes
   b) Straight binary code
   c) Gray code
   d) Error code
2. An n variable k map can have
   a) n^2 cells
   b) n^n cells
   c) n^{2n} cells
   d) 2^n cells
3. In 32:1 multiplexer the number of select lines are
   a) 5
   b) 3
   c) 4
   d) 6
4. The parity check circuit checks the
   a) Even or odd number of ‘O’s in a binary sequence
   b) Even or odd number of ‘1’s in the binary sequence
   c) Even number of ‘X’s in a binary sequence
   d) Both a & b
5. Synchronous counters eliminate the delay problems encountered with asynchronous (ripple) counters because the
   a) input clock pulses are applied only to the first and last stages
   b) input clock pulses are applied only to the last stage
   c) input clock pulses are not used to activate any of the counter stages
   d) input clock pulses are applied simultaneously to each stage

6. A basic S-R flip-flop can be constructed by cross-coupling which basic logic gates?
   a) AND or OR gates
   b) XOR or XNOR gates
   c) NOR or NAND gates
   d) AND or NOR gates
7. How many flip-flops are required to make a MOD-32 binary counter?
   a) 3
   b) 32
   c) 5
   d) 6
8. How is a *J-K* flip-flop made to toggle?
   a) $J = 1, K = 1$
   b) $J = 0, K = 1$
   c) $J = 1, K = 0$
   d) $J = 0, K = 0$
9. Which of the following is the fastest logic?
   a) TTL
   b) CMOS
   c) ECL
   d) LSI
10. The difference between a PLA and a PAL is
   a) The PLA has a programmable OR plane and a programmable AND plane, while the PAL has a programmable AND plane only.
   b) The PAL has a programmable OR plane and a programmable AND plane, while the PLA has a programmable AND plane only.
   c) The PAL has more possible product terms than the PLA
   d) PALs and PLAs are the same thing.

PART B (10 x 2 = 20 Marks)

11. Given the two binary numbers X = 1010100 and Y = 1000011, perform the subtraction a) X-Y and (b) Y-X using 2's complements.
12. Prove that ABC + ABC' +AB'C + A'BC = AB + AC + BC
13. Assume that the exclusive-OR gate has a propagation delay of 10 nanoseconds and the AND and OR gates have a propagation delay of 5 nanoseconds. What is the total propagation delay time in the 4-bit Ripple Carry Adder?
14. How is a combinational circuit different from a sequential circuit?
15. Write the characteristic table and equation of SR flip-flop.
16. Give the differences between Mealy and Moore model.
17. When does a race around condition occur? How is it overcome?
18. Draw the block diagram for a Master-Slave JK flipflop.
19. List the characteristics of Digital Logic Families.
20. Why TTL is preferred over DTL?

PART C (5 x 14 = 70 Marks)

21. a) Determine the prime-implicants of the Boolean function by using the tabulation method.

F(A, B, C, D) = ∑(1, 3, 4, 5, 10, 11, 12, 13, 14, 15)

(OR)

b) The following truth table describes a three-input combinational logic function:

a b c z

0 0 0 0

0 0 1 1

0 1 0 0

0 1 1 0

1 0 0 0

1 0 1 1

1 1 0 1

1 1 1 1

Write down a Boolean expression for the output of this function in sum of products form. Can your expression be reduced to a simpler sum of products form? What are the advantages and disadvantages of sum of products circuits for implementing combinational logic functions?

22. a) Design a circuit that compares two 3-bit numbers and explain how it determines their relative magnitudes.

(OR)

b) (i) Design a combinational circuit that converts binary information from *n* input lines to a maximum of 2^n unique output lines and explain the same. (7)

(ii) Implement the following Boolean Function using 4:1 MUX. (7)

F(A,B,C,D) = ∑m(0,1,2,4,6,9,12,14)

23. a) Design a MOD-6 synchronous Sequential Counter Synthesis using J-K Flip flop.

(OR)

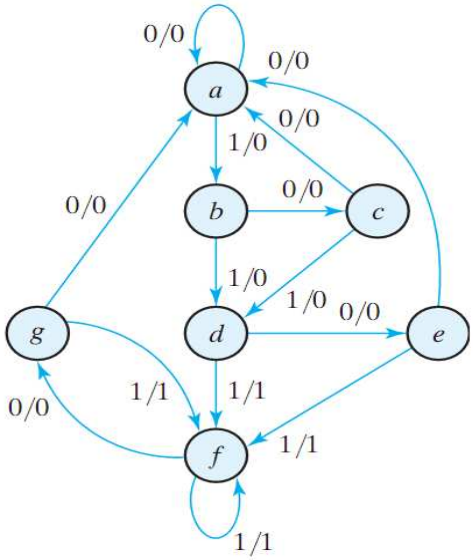
b) Explain BCD counter with neat a diagram.

24. a) (i) Illustrate the operation of universal shift register with neat diagram. (8)

(ii) Explain how hazard free realization can be obtained for a Boolean Function. (6)

(OR)

b) Reduce the number of states in the following state diagram and tabulate the reduced state table.



25. a) (i) With a neat diagram explain the working of (a) Multiplexer with transmission CMOS gates. (b) Gated D-latch with transmission CMOS gates. (7)

(ii) Design a TTL gate with totem pole output circuit and analyze the functionality of the circuit. (7)

(OR)

b) Implement the switching function.

Z1 = ab'd'e +a'b'c'd'e' + bc + de

Z2 = a'c'e

Z3 = bc + de + c'd'e' + bd

Z4 =a'c'e + ce

using a 5 x 8 x 4 PLA

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