KUMARAGURU
college of technology
character is life

Register Number:…….

B.E DEGREE EXAMINATIONS: DEC 2014

(Regulation 2009)

Third Semester

ELECTRONICS AND COMMUNICATION ENGINEERING

ECE105: Electronic Circuits I

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. The biasing circuit for BJT amplifier ensures that the operating point lies
   a) In the saturation region
   b) In the cut-off region
   c) In the active region
   d) Within maximum power dissipation curve
2. The maximum current, $I_{DSS,}$ in JFET results when
   a) $V_{GS} = 0$
   b) $V_P = 0$
   c) $V_{GS} = V_P/2$
   d) $V_{GS} = V_P$
3. In a CE voltage-divider bias circuit, the voltage gain Av, in terms of 'h' parameters, is given approximately as
   a) Av = hfe / hie
   b) Av = - hfe / hie
   c) Av = - (hfe / hie) . Rc
   d) Av = (hfe / hie) . Rc
4. The trans-conductance, gm, in a FET amplifier relates
   a) Ids, Vgs
   b) Ids, Vds
   c) Ids, V_G
   d) Ids, V_{DD}
5. A cascode amplifier is a combination of
   a) CE - CC
   b) CE - CB
   c) CB - CC
   d) CC - CB

6. If β1, β2 are gain of two transistors respectively, in a Darlington configuration, the total current gain is

   a) β1 + β2 b) 2. β1. β2

   c) β1.β2 d) 2. (β1 + β2)

7. In a Class B power amplifier, the conduction cycle of each transistor is

   a) 0◦ b) 90◦

   c) 180◦ d) 270◦

8. The main application of Class C amplifier is in

   a) Carrier amplifier b) IF amplifier

   c) Wide band amplifier d) RF amplifier

9. The output voltage of a full wave rectifier is

   a) Vdc = 0.318Vm b) Vdc = 0.636Vm

   c) Vdc = 0.308Vm d) Vdc = Vm

10. A 100 µF capacitor is connected across a full wave rectifier that delivers a load current of 50 mA. The value of ripple voltage is

    a) 1 V b) 1.2 V

    c) 2 V d) 2.4 V

PART B (10 x 2 = 20 Marks)

11. State the main objective of biasing a BJT.
12. A fixed bias circuit operates with a power supply voltage of 12V. Determine the quiescent values of Ic and V_{CE} if R_B = 240 KΩ and R_C = 2.2 KΩ. Assume β = 50.
13. Draw the small signal h-parameter model for a CE amplifier.
14. What is the purpose input resistor R1 and R2 in a voltage-divider bias circuit of JFET-CS configuration?
15. What is the effect on bandwidth due to cascaded multi-stage amplifiers?
16. Define CMRR. What is its significance?
17. What is the need for Class AB configuration?
18. What is thermal resistance?
19. Define voltage regulation.

20. What are the advantages of SMPS over conventional power supplies?

PART C (5 x 14 = 70 Marks)

21. a) i) A CE amplifier uses voltage divider bias with the following component values: R1 = 39 KΩ, R2 = 3.9 KΩ, Rc = 10 KΩ, R_E = 1.5 KΩ, Cc= 10 µF and C_E = 50 µF. Assuming β = 100, calculate Ic_Q and V_{CQ}. Draw the circuit. Use of graphical method is optional. (V_{CC} = 15v) (10)

ii) What are the factors that affect the stability of operating point? Explain with respect to CE configuration. (4)

(OR)

b) i) A CS-JFET amplifier uses voltage divider bias with the following component values: R1 = 2.1MΩ, R2 = 270 KΩ, R_D = 2.4 KΩ, R_S = 1.5 kΩ, Cc= 5 µF and C_s= 20 µF. If I_{DSS} = 8 mA and Vp = -4V. Obtain quiescent values for I_D and V_{DS}. Use of graphical method. (Hint: Use Schockley equation). (V_{DD} = 18v) (10)

ii) Illustrate the effect of changing values of R_S in the load line on quiescent point. Use transfer curve of CS-JFET configuration. (4)

22. a) i) A BJT CE small signal amplifier has hfe = 200. Determine small signal voltage gain, current gain, input impedance and output impedance. The component values are R1 = 120 kΩ, R2 = 27 kΩ, Rc = 6.8 kΩ and gfe = 40 mS. (V_{CC} = 15v) (10)

ii) Draw and explain hybrid-Π model for small signal CE amplifier. (4)

(OR)

b) i) Compare performance characteristics of CS, CG and CD configurations of FET amplifiers. (10)

ii) Discuss the high frequency response of CS-JFET amplifier. (4)

23. a) i) What is the advantage of cascade connection? Draw the circuit of a (7)

typical cascade amplifier and explain.

ii) Illustrate how constant current source improves CMRR in a differential amplifier. Use circuit schematics. (7)

(OR)

b) i) Draw and explain the circuit of a two-stage RC coupled amplifier. Also, highlight the design considerations that need to be taken care of. (10)

ii) Derive an expression for overall bandwidth for a n-stage cascaded amplifier. (4)

24. a) i) Describe how a transformer coupled class A amplifier achieves a maximum efficiency of 50%. (10)

ii) What is cross-over distortion? How is it avoided? (4)

(OR)

b) i) Explain the working of complementary-symmetry push- pull class B amplifier. (10)

ii) What is the significance of thermal resistance for power transistor? Explain. (4)

25. a) i) Compare the performance of half-wave, full-wave and bridge rectifiers. (10)

ii) Write short notes on SMPS. (4)

(OR)

b) (i) Describe the operation of BJT series voltage regulator. (7)

ii) What is the role of capacitor in a filter? Explain with respect to full-wave rectifier. (7)

****