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Register Number: ……………………

B.E DEGREE EXAMINATIONS: NOV/DEC 2014

(Regulation 2009)

Fifth Semester

ELECTRONICS AND COMMUNICATION ENGINEERING

ECE112 : Computer Architecture

Time: Three Hours   **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. The 2's complement of binary value 1101100 is
   a) 0010011
   b) 0010010
   c) 0010100
   d) 1101101

2. The transfer of information from a memory word to the outside environment is called
   a) Write operation
   b) High impedance
   c) buffer
   d) Read operation

3. _____ handles both negative and positive multipliers uniformly.
   a) booth algorithm
   b) fast multiplier
   c) sequential multiplier
   d) carry save addition

4. Bit-pair recording halves the maximum number of _____
   a) 1's
   b) summands
   c) 0's
   d) carry

5. The process of physically removing the chip from the circuit for reprogramming and that its entire contents are erased by the ultraviolet signal is in
   a) ROM
   b) PROM
   c) EPROM
   d) EEPROM

6. TLB is
   a) Translation Lookaside Buffer
   b) Translation Lower side Buffer
   c) Transfer Lookaside Buffer
   d) Transfer Lower side Buffer

7. Which technique provides a substantial improvement in performance by overlapping the execution of successive instructions?

a) Multiple buses   b) multiprocessor

c) pipelining   d) superscalar operation

8. The UltraSPARC II has a _____ stage instruction pipeline.

a) Three   b) Five

c) Two   d) Nine

9. All devices waiting to use the bus have equal responsibility in carrying out the arbitration process, without using a central arbiter is called

a) Bus arbitration   b) Centralized arbitration

c) Start arbitration   d) Distributed arbitration

10. When operands are brought into the processor, they are stored in high-speed storage elements called _____

a) cache   b) program counter

c) MDR   d) registers

PART B (10 x 2 = 20 Marks)

11. How overflow is detected in fixed point numbers.

12. Let X=1010100 and Y=1000011, perform X-Y and X-Y using 2's complement.

13. Perform an addition with two numbers (11010 and 11100) using full adder circuit and display an array of carry values.

14. What are the two techniques to speed up the multiplication operation?

15. Differentiate SRAM from DRAM.

16. Write the structure of memory hierarchy.

17. Name the factors that affect the pipeline performance.

18. What is the drawback of micro programmed control?

19. What are the various mechanisms for implementing I/O operations?

20. Why does DMA have priority over the CPU when both request a memory transfer?

PART C (5 x 14 = 70 Marks)

21. a) (i) Discuss the shift micro operations and control operations of computer. (7)

       (ii) Draw and explain IEEE standard single precision and double precision floating point format. (7)

(OR)

b) (i) Describe the general approach for register level systems design with an example. (7)

       (ii) How will you perform arithmetic and logic micro operations? (7)

22. a) (i) Reproduce Booth's algorithm for two's complement multiplication and illustrate (7) the algorithm with an example.

    (ii) With suitable diagram, examine how multiplication can be performed using a (7) multistage carry-save adder circuit and also the implementation of a pipelined carry-save multiplier.

(OR)

    b) (i) Illustrate the working principle of fast adders and elaborate its components. (7)

    (ii) Compare and contrast the concept of Signed operand multiplication and fast (7) multiplication.

23. a) (i) Give the basic cell of an associative memory and explain its operation. (7)

    (ii) Explain the virtual memory address translation and TLB with necessary (7) diagram.

(OR)

    b) Give the structure of semiconductor RAM memories. Explain the read and write operations in detail.

24. a) (i) Give the organization of typical hardwired control unit and explain the functions (8) performed by the various blocks.

    (ii) Explain the multiple bus organization in detail. (6)

(OR)

    b) Discuss the various hazards that might arise in a pipeline. What are the remedies commonly adopted to overcome/minimize these hazards?

25. a) Explain the functions performed by a standard I/O interfaces with bus standards.

(OR)

    b) (i) Describe the data transfer method using DMA. (7)

    (ii) Explain in detail about interrupt handling. (7)

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