KUMARAGURU
college of technology
character is life

Register Number:……..

B.E DEGREE EXAMINATIONS: NOV/DEC 2014

(Regulation 2009)

Seventh semester

ELECTRONICS AND INSTRUMENTATION ENGINEERING

EIE117: VLSI Design

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. Most small-signal E-MOSFETs are found in
   a) Heavy-current applications b) Disk drives
   c) Discrete circuits d) Integrated circuit
2. The main advantage of CMOS is its
   a) High power rating b) Switching capability
   c) Small-signal operation d) Low power consumption
3. Bi-CMOS gates can be used to improve
   a) Power dissipation b) The performance of line driver
   c) Propagation delay d) Output impedance
4. NMOS 4 to1 MUX has
   a) Faster fall time b) Faster rise time
   c) Slow rise time d) Slow fall time
5. The two phase clock is required for
   a) PLA b) FSM
   c) FPLA d) DLA
6. A ratioed logic which uses a grounded pMOS load is referred as a_____ gate
   a) pSeudo-nMOS b) Dynamic CMOS
   c) Static CMOS d) Clocked nMOS
7. In NMOS PLA
   a) only AND array is programmable b) only OR array is programmable
   c) both OR & AND array are programmable d) macro cell is the building block.

8. LUT is used in

a) CPLD b) ASIC

c) FPGA d) SPLD

9. VHDL is a

a) Multithread program b) A programming language like C

c) Single user program d) Sequential program

10. In VHDL, sequential statements are defined in the

a) architecture b) process

c) package d) Function

PART B (10 x 2 = 20 Marks)

11. Write down the equation for describing the channel length modulation effect in nMOS transistors.
12. What is body effect?
13. Draw the equivalent circuit for operating region C of CMOS inverter.
14. Draw the nMOS noninverting tristable super buffer.
15. Design an AOI Logic Circuit for the SOP logic expression $F = \overline{A}\,B\,\overline{C}\,D + B\,C\,\overline{D} + A\,\overline{B}$
16. Implement 4X1 MUX using CMOS transmission gate.
17. Draw the basic floor plan of a nMOS PLA structure.
18. Compare antifuse with SRAM.
19. Write down a typical test bench format
20. Write the VHDL code to implement Half Adder logic.

PART C (5 x 14 = 70 Marks)

21. a) (i) Explain photolithography, gate/source/drain formation and isolation steps of CMOS fabrication process with neat diagrams. (8)

(ii) Draw the schematic and Physical design of 2 input CMOS NAND gate. (6)

(OR)

b) (i) Explain in detail about the electrical model of a MOS transistor. (6)

(ii) Discuss in detail about the ideal VI characteristics of MOS device. (8)

22. a) Draw the stick diagram and mask layout for a CMOS two input NOR gate and stick diagram of two input NAND gate.

(OR)

b) (i) Determine the pull up and pull down ratio for an nMOS inverter driven through one or more pass transistor. (12)

(ii) What are λ based design rule? (2)

23. a) (i) Realize the function f= ∑m(3,7,11,12,13,14,15)+ ∑d(6,9) in a CMOS circuit in all four possible combination of SOP and POS gates. (7)

(ii) Describe the basic principle of operation of dynamic CMOS,domino logic with neat diagrams. (7)

(OR)

b) (i) Draw the circuit diagram for 4-by-4 barrel shifter using complementary transmission gates and explain its shifting operation. (7)

(ii) Design 3 input tally circuit using pass transistor logic. (7)

24. a) (i) Realize NMOS NOR-NOR and NMOS NAND-NAND PLA. (7)

(ii) Realize precharged NMOS NOR-NOR PLA and NMOS NAND-NAND PLA. (7)

(OR)

b) Minimize the four functions W,X,Y and Z and realize a minimum sized PLA to implement them. The d_i are don't care minterms.

W = ∑m(4,5,8,14)+ d(15)

X= ∑m(1,8,14,15)+d(5)

Y =∑m(4,5,8,14,15)

Z=∑m(1,3,5,11,15)+d(14)

25. a) (i) Design and develop the HDL project to realize the function of a BCD counter using any one model. (7)

(ii) Write a VHDL program for signed comparator. (7)

(OR)

b) (i) Design and develop the HDL project to realize the function of a carry ripple adder using any one model. (7)

(ii) Write a VHDL program for encoder. (7)

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