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Register Number:……..

B.E/B.TECH DEGREE EXAMINATIONS: NOV / DEC 2014

(Regulation 2009)

Fourth Semester

ITY 102: MICROPROCESSORS

(Common to CSE and IT)

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. Auxiliary carry flag holds
   a) Carry out of bit 3 to 4
   b) Carry out of bit 6 to 7
   c) Carry out of bit 7 to 8
   d) Carry out of bit 7 to carry bit
2. Intel 8085 can handle a memory capacity of
   a) 8 bits
   b) 1 MB
   c) 16 bits
   d) 64 KB
3. Rotate Accumulator Right belongs to
   a) Machine control, two byte instruction group
   b) Logical, single byte instruction group
   c) Machine control, single byte instruction group
   d) Logical, two byte instruction group
4. Compare Memory with accumulator works on
   a) Direct Addressing mode
   b) Immediate Addressing mode
   c) Indirect addressing mode
   d) Implicit Addressing mode
5. Handshaking mode of data transfer is also called
   a) Serial data transfer
   b) Synchronous data transfer
   c) Asynchronous data transfer
   d) Parallel data transfer
6. In mode 1 of 8253 timer, the trigger signal is given as
   a) High to Low applied to OUT
   b) Low to High applied to GATE
   c) High to Low applied to GATE
   d) Low to High applied to OUT

7. When the signal READY in 8086 is high, it indicates that
   a) The processor is ready to transfer data
   b) The processor is ready to receive data
   c) The peripheral is ready to transfer data
   d) The peripheral is ready to receive data
8. BHE in conjunction with A0 decides
   a) The length of the data to be transferred
   b) The destination as memory or I/.O
   c) The type of data to be transferred
   d) The source of data as memory or I/O
9. Coprocessors are used to
   a) Take up complicated and time consuming processes
   b) Interface the processor with a peripheral
   c) Reduce the speed of the microprocessor
   d) Handle the interrupts
10. Interrupts are not allowed to interrupt the
   a) Data transfer between memory and processor
   b) Complicated processes
   c) DMA process
   d) Critical section of the code

PART B (10 x 2 = 20 Marks)

11. Explain about program status word of Intel 8085.
12. A microprocessor takes n microseconds for executing an instruction. What design change will make the microprocessor to execute the same instruction in n/2 microseconds?
13. What is the significance of XCHG and SPHL instructions?
14. Applying the Jump if Zero control, write a decrease count loop in 8085 assembly language.
15. Compare the burst mode and cycle stealing DMA techniques.
16. Assume that multiple keys are pressed simultaneously in a computer. How does a key board controller handle this?
17. Compare the minimum and maximum mode of 8086.
18. With the template structure explain the process of building up the opcode for 8086.
19. Draw the structure of status register of 8087 numeric coprocessor and explain the bits.
20. For 8086 based multiprocessor system, compare closely coupled and loosely coupled configurations.

PART C (5 x 14 = 70 Marks)

21. a) (i) How are the address and data lines demultiplexed in 8085? (6)

(ii) Draw the schematic for process flow in a microprocessor and explain how an instruction is executed. (8)

(OR)

b) (i) List the interrupts available in 8085 microprocessor with their applications. (7)

(ii) Draw the timing diagram for I/ O read and Explain. (7)

22. a) (i) List various instructions that can be used to clear accumulator in 8085 microprocessor. (4)

(ii) Assume register B holds 93H and the accumulator holds 15H.Illustrate the results of the instructions ORA B, ADC B, XRA B and CMA. (10)

(OR)

b) (i) What are RIM and SIM instructions and where are they used? (4)

(ii) How many times the given loop will be executed? What will be the contents of HL reg.pair when the program control reaches to HLT instruction? (10)

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        MVI A, 00H
        LXI H, 5300H
LOOP:   DCX H
        DCR A
        JNZ LOOP
        HLT
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23. a) (i) How much current is needed to drive an LED? Draw typical driver circuit for it and explain. (7)

(ii) Explain the working of receiver part of a USART. (7)

(OR)

b) (i) What is the internal operating frequency of 8279? How can you derive it from any available clock signal? (4)

(ii) What are the modes of operation supported by 8255? (10)

24. a) Explain the pipeline operation in 8086. (4)

Write a program using 8086 assembly language to move N number of bytes from the location starting at ‘OLDLOC’ to the location starting at ‘NEWLOC’. Algorithm steps are required. (10)

(OR)

b) List the ways in which the effective address be calculated by the addressing modes in 8086? (4)

Explain with examples the addressing modes of 8086 processor. (10)

25. a) Draw the schematic representation of 8086 CPU working in the maximum mode and explain the function of the components involved.

(OR)

b) (i) Draw a loosely coupled configuration of 8086 processor and explain the signals. (8)

(ii) Describe about Pentium architecture. (6)

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