KUMARAGURU
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Register Number: …….

B.E DEGREE EXAMINATIONS: NOV/DEC 2014

(Regulation 2013)

Third Semester

ELECTRONICS AND COMMUNICATION ENGINEERING

U13ECT301:Digital Electronics

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. Identify the number of gates required for implementing the expression,Y=AB+BC+AC
   a) 6 b) 5
   c) 4 d) 3
2. The two's complement of $(10110)_2$ is……..
3. What is the odd and even parity bit for a 3 bit message 110?
   a) 0&1 b) 1&0
   c) 0&0 d) 1&1
4. …… is a circuit which uses a binary decoder to direct a digital signal from several source to one of the several outputs.
5. A MOD-4 Counter will count from
   a) 0 to 4 b) 0 to 3
   c) Any number n to n+4 d) None of above
6. ……. Flipflop is used to avoid Race around Condition.
7. The hazards occurs only in
   a) Counters b) Shift Registers
   c) Asynchronous Circuits d) Synchronous Circuits
8. …….. shift register can be used to construct a Johnson Counter.
9. How many 1024x1 RAM chips are needed to construct a 1024x 8 memory system?
   a) 3 b) 4
   c) 8 d) 6
10. The volatile memory is ……..

PART B (10 x 2 = 20 Marks)

(Not more than 40 words)

11. Simplify the expression, f(A,B,C)=∑(0,2,3,6) using K-map.
12. State the advantage of Gray code over Binary Code?
13. Define Ripple Carry Adder with suitable diagram.
14. Define Propagation Delay of a Gate.
15. Distinguish between Combinational and Sequential Circuit.
16. Examine the number of flipflops necessary to construct a MOD-13 Counter.
17. What is meant by Universal Shift Register?
18. Distinguish between Static and Dynamic Hazard.
19. How many address lines are needed to access a 1024x8 RAM?
20. Compare the TTL,ECL and CMOS digital logic families.

PART C (5 x 14 = 70 Marks)

(Not more than 400 words)

Q.No. 21 is Compulsory

21. Design a Synchronous MOD-10 Counter using JK Flipflop

22. a) (i) Compute the given Boolean Function using K-Map f(A,B,C,D,E)= ∑(0,2,4,6,9,13,21,23,25,29,31) (10)

(ii) Simplify the expression,y=AB+A'C+AB'C(AB+C) using Boolean Algebra. (4)

(OR)

b) (i) Compute the given Boolean function using Tabulation method f(w,x,y,z)=∑(1,4,6,7,8,9,10,11,15). (10)

(ii) Discuss about Prime implicant and Essential Prime Implicant with suitable examples (4)

23. a) (i) Construct a Full Adder using two Half Adders (6)

(ii) Construct the given function ,F(A,B,C,D)=∑(0,1,3,4,8,9,15) using Multiplexer and draw the logic diagram. (8)

(OR)

b) (i) What is an Encoder? Design a Decimal to BCD Encoder with suitable diagrams (10)

(ii) Explain the 4-bit Adder/Subtractor with neat diagrams (4)

24. a) (i) Explain about Serial-In Parallel-Out Shift register with suitable diagrams. (4)

(ii) Discuss about the state Reduction and state assignment techniques with suitable examples. (10)

(OR)

b) (i) Explain about static and dynamic hazards with suitable diagrams (8)

(ii) Design a Hazard-free circuit for the function, $F(w,x,y,z)=\sum(0,2,6,7,8,10,12)$. (6)

25. a) (i) Enumerate about ROM and RAM with neat diagrams. (9)

(ii) Draw the logic Construction of 32x 4 ROM. (5)

(OR)

b) (i) Implement the given two Boolean functions,$F1(A,B,C)=\sum(0,1,2,4)$ $F2(A,B,C)=\sum(0,5,6,7)$ using PLA. (7)

(ii) Outline the open-Collector output of Transistor-Transistor Logic Gate. (7)

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