KUMARAGURU
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Register Number: …….

B.TECH DEGREE EXAMINATIONS: NOV/DEC 2014

(Regulation 2013)

Third Semester

INFORMATION TECHNOLOGY

U13ITT302: Digital Systems And Design

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. Which of following consume minimum power?
   a) TTL. b) CMOS.
   c) DTL. d) RTL
2. An open collector output can _____ current, but it cannot _____.
3. A Multiplexer with four select bits is a
   a) 4:1 Multiplexer b) 8:1 multiplexer
   c) 16:1 Multiplexer d) 32:1 Multiplexer
4. A multiplexer is also known as ……..
5. A sequential circuit does not use clock pulses. It is
   a) an asynchronous sequential circuit b) a synchronous sequential circuit
   c) a counter d) a shift register
6. How many flip-flops are required to make a MOD-32 binary counter?
7. In a JK Flip-Flop, toggle means
   a) Set Q = 1 and Q = 0. b) Set Q = 0 and Q = 1.
   c) Change the output to the opposite state. d) No change in output.
8. If even parity mechanism is being used in system using ASCII code for data transfer then incorrect receipt of data byte is _____.
9. How many inputs and outputs does a full adder have?
   a) Two inputs, one output. b) Two inputs, two output.
   c) Two inputs, three output. d) Three inputs, two output
10. A group of 8 bits is known as_____.

PART B (10 x 2 = 20 Marks)

(Not more than 40 words)

11. Define duality property.
12. State the limitations of Karnaugh map.
13. Write down the steps in implementing a Boolean function with levels of NAND Gates?
14. Why are NAND and NOR gates known as universal gates?
15. What is a programmable logic array? How does it differ from ROM?
16. Give the comparison between combinational circuits and sequential circuits.
17. What is race around condition?
18. List various types of flip-flop.
19. What is meant by modulus of a counter?
20. A counter has 14 stable states 0000 through 1101. If the input frequency is 50 KHz what will be its output frequency?

PART C (5 x 14 = 70 Marks)

(Not more than 400 words)

Q.No. 21 is Compulsory

21. (i) What is PAL? How does it differ from PLA? (7)

    (ii) Implement the functions: X = A'BC + ABC + A'B'C' and Y = ABC + AB'C using a PLA. (7)

22. a) (i) Design a logic circuit that accepts a 4-bit Grey code and converts it into 4-bit binary code. (10)

    (ii) Draw the logic diagram of a full subtractor using half subtractors and explain its working with the help of a truth table. (4)

(OR)

    b) (i) Express the Boolean function F =A+B’C in sum of minterms (4+4)

    Express the Boolean function F=xy+x’z in production of maxterms.

    (ii) In what way is the Quine-McCluskey method advantageous over the karnaugh method of simplifying a Boolean function? (6)

23. a) Draw the circuit for 3-to-8-decoder and implement the functions

    F1 (A, B, C) =II (0, 1, 3, 7)

    F2 (A, B, C) =II (2, 3, 7) using a 3-to-8-decoder

(OR)

b) (i) Describe the operation of 8:1 multiplexer using functional block diagram. (8)

(ii) What is a demultiplexer? Discuss the differences between a demultiplexer and a decoder. (6)

24. a) Draw the state diagram, characteristic table and characteristic equations of T, D and JK Flip flop.

(OR)

b) (i) How race around condition can be eliminated? (7)

(ii) What is Shift register? What are the types of register? Explain any one-Shift register with example. (7)

25. a) Write short notes on state reduction and state assignment in Sequential circuit design.

(OR)

b) (i) How is it possible to make a modulo 2n counter using N-flip-flops? Name the two types of such counters. (6)

(ii) Design a 2-bit synchronous counter using JK flip flops. (8)

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