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Register Number:……….……

M.E DEGREE EXAMINATIONS: JAN 2015

(Regulation 2014)

First Semester

COMPUTER SCIENCE AND ENGINEERING

P14CST102 : High Performance Computer Architecture

Time: Three Hours   **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. The clock rate of the processor can be improved by   [K₁]
    1. Improving the IC technology of the logic circuits
    2. By using overclocking method
    3. Reducing the amount of processing done in one step
    Which of these statements are correct?

    a) 1,3   b) 3
    c) 1,2,3   d) 2,3

2. SPEC stands for   [K₁]
    a) Standard Performance Evaluation Code   b) System Processing Enhancing Code
    c) System Performance Evaluation   d) Standard Processing Enhancement
        Corporation   Corporation

3. Consider the following statements: [K₃]
    1. Pipelining strategy is used to implement instruction execution
    2. It is used for instruction decoding
    3. It can also be used for instruction prefetching
    4. Used for instruction manipulation
    Which of these statements are correct?
    a) 2,4   b) 4
    c) 3   d) 1,3

4. Assertion (A) : An optimizing compiler takes advantage of the type of processor and reduces its   [K₂]
    process time
    Reason (R) : Compilers make assumptions about the ability of later steps to deal with certain
    issues
    a) Both A and R are true ; R is the correct   b) A is true and R is false
        explanation of A
    c) Both A and R are true ; R is not the   d) R is true and A is false
        correct explanation of A

5. The steps through which every instruction goes is   [K₁]
   1. Execute
   2. Issue operands
   3. Write result
   The correct sequence is
   a) 2-1-3   b) 1-2-3
   c) 3-2-1   d) 3-1-2

6. Which one of the following is not a valid state of a thread?   [K₁]

   a) parsing   b) running

   c) blocked   d) ready

7. Match list I with list II and select the correct answer using the codes given below: [K₃]
              List I   List II
   1). Machines that store operands in pushdown stack.   A. addressing modes
   2). The different ways in which the location of an
        operand is specified in an instruction   B. Register mode
   3). The operand is the contents of a processor register   C. zero addresses instructions
   a) 1.C, 2.A, 3.B   b) 1.A, 2.C, 3.B

   c) 1.C, 2.B, 3.A   d) 1.B, 2.A, 3.C

8. Consider the following statements: [K₁]
   The purpose of RAID system is to
   1. increase the processor speed
   2. increase the disk storage capacity and availability
   3. increase the operating system efficiency
   4. decrease operating system efficiency
   Which of these statements are correct?
   a) 1   b) 2,4
   c) 3,4   d) 2

9. The extra time needed to bring the data into memory in case of a miss is called as   [K₂]

   a) Delay   b) Propagation time

   c) Miss rate   d) Miss penalty

10. The method of synchronizing the processor with the I/O device in which the device sends a   [K₃]
    signal when it is ready is
    a) Interrupts   b) Exceptions

    c) DMA   d) Signal handling

PART B (10 x 2 = 20 Marks)

11. List and define the two measures of dependability.   [K₁]

12. What is locality of reference? Classify the types of locality of references. [K₂]

13. What are the assumptions made for a perfect processor in the hardware speculation? [K₂]

14. What are the advantages of dynamic scheduling? [K₁]

15. Tell the limitations of multiple issue processors? [K₂]

16. What do you mean by multithreading? [K₁]

17. Tell why multiprocessors are often called as message passing multiprocessors? [K₂]

18. When do you say that a program is synchronized? [K₁]

19. Differentiate cache memory from virtual memory [K₂]

20. Define: dirty bit and miss penalty [K₁]

PART C (6 x 5 = 30 Marks)

21. How do you measure the performance of a computer? Discuss about the levels of programs used to evaluate the performance. [K₂]

22. Define Amdahl's law with a formula to calculate the overall speedup. Also mention the factors to measure speedup using Amdahl's law. [K₅]

23. Define pipelining? Create a simple implementation of pipeline processor and explain how it allows every instruction to be executed in 4 clock cycles. [K₆]

24. Define instruction level parallelism. Discuss about the limitations of ILP for related processors? [K₂]

25. What are the ways of measuring the performance of symmetric shared-memory multiprocessor? Explain. [K₂]

26. Explain about Reliability measures and Benchmarks [K₂]

PART D (4 x 10 = 40 Marks)

27. Describe how you overcome data hazards with Dynamic scheduling approach. [K₂]

28. What is multithreading? Discuss about how it uses ILP support to exploit thread level parallelism. [K₆]

29. Demonstrate the working of Directory based cache coherence protocol in detail. [K₃]

30. How do you optimize the performance of Cache memory? Explain. [K₂]

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