KUMARAGURU college of technology
character is life

Register Number: ……..

B.E DEGREE EXAMINATIONS: MAY 2015

(Regulation 2009)

Fifth Semester

ELECTRONICS AND COMMUNICATION ENGINEERING

ECE112:Computer Architecture

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. Negative numbers cannot be represented in
   a) Signed magnitude form
   b) 1's complement form
   c) 8-4-2-1 code
   d) 2's complement form
2. To divide the binary number by 2
   a) Left shift the number once
   b) Right shift the number twice
   c) Right shift the number once
   d) Left shift the number twice
3. In addition of two signed numbers, represented in 2' s complement form generates an overflow if
   a) A. B = 0
   b) A + B = 1
   c) A (XOR) B = 1
   d) A = 0
4. It is important to retain extra bits during manipulation of binary numbers to yield maximum accuracy, these bits are called
   a) Guard bits
   b) Chopping bits
   c) Extra bits
   d) Binary bits
5. The number of 128 X 8 RAM chips required to build a memory capacity of 2048 bytes
   a) 8
   b) 16
   c) 24
   d) 32
6. In a virtual memory system, the addresses used by the programmer belongs to
   a) physical addresses
   b) Main memory address
   c) memory space
   d) address space
7. If an exception occurs during an instruction execution, all subsequent instructions that may have been partially executed are discarded, called as
   a) Imprecise exception
   b) Pipelining
   c) Precise exception
   d) Inorder exception

8. WAW hazards are eliminated using

a) Out of order execution
b) Speculation
c) Register remaining
d) Branch prediction

9. In a non-vectored interrupt, the address of interrupt service routine is

a) Supplied by the interrupting I/O device
b) Assigned to a fixed memory location
c) Obtained through Vector address generator device
d) Obtained from interrupt address table

10. The ---------- controller acts as an initiator contents for the control bus

a) SCSI
b) ISB
c) USB
d) PCI

PART B (10 x 2 = 20 Marks)

11. Why floating point number is more difficult to represent than fixed point number?
12. What is the use of control functions?
13. How is a carry look-ahead adder faster than a ripple carry adder?
14. Summarize the significant features of Booth's algorithm.
15. List the factors that determine the storage device performance.
16. What is an interleaved memory organization?
17. Distinguish between Hardwired and Micro programmed control.
18. Identify the methods of overcoming the data hazards.
19. Outline the sequence of operations that a processor does on receiving an interrupt call.
20. Compare memory mapped and isolated I/Os.

PART C (5 x 14 = 70 Marks)

21. a) (i) Illustrate with examples the arithmetic micro operations. (8)

(ii) List the basic registers and explain how data are transferred to registers (6)

(OR)

b) (i) Discuss in detail about shift micro operations (7)

(ii) Design a 4–bit binary incrementer. (7)

22. a) (i) Select a proper hardware to be used for addition and subtraction of two decimal numbers in signed magnitude representation. Also examine how overflow is detected. (10)

(ii) Distinguish between Von Neumann and Harvard architecture. (4)

(OR)

b) (i) Develop a flow chart for an algorithm used for division of two floating point numbers. (7)

(ii) Design and explain a 16 bit carry look ahead adder using 4 bit adders (7)

23. a) (i) Outline the structure of memory hierarchy in a digital computer. (6)

(ii) Discuss with necessary block diagram the steps involved in address translation of virtual memory. (8)

(OR)

b) (i) A digital computer has a memory unit of 64K X 16 and a cache memory of 1K words. The cache uses direct mapping with a block size of four words. How many bits are there in the tag, index, block and word fields of the address format? Select the number of blocks the cache can accommodate. (10)

(ii) Discuss on memory management hardware. (4)

24. a) Examine with a suitable example the multi-bus organization for data path.

(OR)

b) (i) Demonstrate the techniques for handling instruction hazards in pipelining. (8)

(ii) Examine the concepts of superscalar operation. (6)

25. a) (i) Explain the need and functions of a typical 8 bit parallel I/O interface. (8)

(ii) Explain the signals exchanged between the CPU and the DMA controller prior to data transfer by the DMA. (6)

(OR)

b) (i) Decide the programming steps required to check when a source interrupts the computer while it is still being serviced by a previous interrupt request from the same source. (7)

(ii) Discuss on the PCI and SCSI bus interface architectures (7)

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