KUMARAGURU college of technology
character is life

Register Number: ……..

**B.E DEGREE EXAMINATIONS: MAY 2015**

(Regulation 2009)

Fourth Semester

**ECE103: DIGITAL ELECTRONICS**

(Common to EEE/EIE)

**Time: Three Hours** **Maximum Marks: 100**

**Answer all the Questions:-**

**PART A (10 x 1 = 10 Marks)**

1. The binary equivalent of hexadecimal number 13AC is

   a) 0001001110101100 b) 0001001110111100

   c) 1001001110111100 d) 1111001110111100

2. The universal gates are

   a) NAND&NOT b) NAND&NOR

   c) AND&NOR d) NAND&OR

3. A combinational circuit is one in which the output depends on

   a) present output and the previous output b) Input combination at that time & previous input combination

   c) Input combination at that time & previous outputs d) Input combination at that time.

4. The Gate ideally suited for Bit Comparison is a

   a) Two input Exclusive OR Gate b) Two input OR Gate

   c) Two input Exclusive NOR Gate d) Two input NOR Gate

5. T Flip flop is used as

   a) Transfer data Circuit b) Transfer clock Circuit

   c) Toggle Switch d) Time Delay Switch

6. The minimum number of flip flops required for a mod-7 ripple Counter are

   a) 4 b) 3

   c) 7 d) 10

7. _____ is a group of flip flops used to store a binary number

   a) Encoder b) Decoder

   c) Multiplexer d) Register

8. If the final stable state that a asynchronous sequential circuit reaches does not depend

on the order in which the state variable changes, then it is called as

a) critical race condition
b) non-critical race condition
c) cycle
d) Hazard

9. The Programmable Array Logic (PAL) has

a) A Programmable AND-array at the input & a fixed OR-array at the output
b) A Fixed AND-array at the input & a Programmable OR-array at the output
c) A Fixed AND-array at the input & a fixed OR-array at the output
d) A Programmable AND-array at the input & a programmable OR-array at the output

10. A ROM is usually not preferred to implement these Boolean functions which

a) are very Complex
b) can otherwise be implemented using a PLA
c) have a large number of 'Don't Care' Conditions
d) have large number of outputs

**PART B (10 x 2 = 20 Marks)**

11. State De Morgan's theorem.
12. Convert the function F(A,B,C,D)= $\prod$ (0,1,2,3,4,6,12) to the other canonical form
13. What are universal gates? Why are they called so?
14. Draw the logic diagram of a half-adder.
15. Differentiate Flip-flops from Latches.
16. What is a race around condition?
17. What is a shift register?
18. What is a critical race?
19. What is the difference between PAL & PLA ?
20. Mention the Characteristics of CMOS.

**PART C (5 x 14 = 70 Marks)**

21. a) (i) Reduce the following Boolean expressions to the indicated number of literals A'B(D'+C'D) + B(A+A'CD)to one literal (5)

(ii) Reduce the following Boolean expressions to the indicated number of literals (A'+C)(A'+C')(A+B+C'D) to four literals (5)

(iii) Implement the Boolean function F = w(x + y + z) + xyz using only NAND gates. (4)

**(OR)**

b) (i) Simplify the boolean function F (*A,B,C,D)*= $\sum$(0,2,3,5,7,8, 10,11,14,15) using K Map (10)

(ii) Implement the Boolean function F= A+CD+(A+D')(C'+D) using gates (4)

22. a) Design a full subtractor circuit with three inputs x, y and z and two outputs D and B.

**(OR)**

b) Design a combinational circuit that converts a decimal digit from BCD to Excess-3 code

23. a) Explain the operation of JK master/slave flip-flops using suitable block diagrams

**(OR)**

b) Explain the operation of mod 8 binary synchronous counter.

24. a) Design a 3 bit Ring Counter and also explain its operation.

**(OR)**

b) (i) What is Hazard? Explain its types (4)

(ii) Give Hazard-free realization for the following Boolean function. (10)

$$F(A,B,C,D) = \sum m(0,2,6,7,8,10,12)$$

25. a) Implement the following Boolean functions using i)ROM and ii)PLA.

$V_2 = \Sigma m(1,2,3,4)$

$V_1 = \Sigma m(2,6,7)$

$V_0 = \Sigma m(4,6,7)$

**(OR)**

b) Implement BCD to Gray Code Converter using PAL

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