



B.E DEGREE EXAMINATIONS: APRIL 2015

(Regulation 2009)

Seventh Semester

ELECTRONICS AND INSTRUMENTATION ENGINEERING

EIE117: VLSI Design

Time: Three Hours

Maximum Marks: 100

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. Which one of these is a weak inversion region in MOSFET?
 - a) Cut-off
 - b) Saturation
 - c) Non-saturated
 - d) None
2. Arranging atoms in a single crystal fashion upon a single crystal substrate is called as _____
 - a) Ion implantation
 - b) Diffusion
 - c) Deposition
 - d) Epitaxy
3. How many transistors are required to fabricate IC7404?
 - a) 8
 - b) 24
 - c) 16
 - d) 32
4. Which color is used to indicate the presence of n-diffusion
 - a) Yellow
 - b) Blue
 - c) Pink
 - d) Green
5. How many output lines for a 1 input tally circuit?
 - a) 3
 - b) 1
 - c) 2
 - d) 4
6. A dynamic CMOS circuit eliminates _____ penalty of static CMOS.
 - a) Power
 - b) Speed
 - c) Area
 - d) Storage
7. In PLA which array is programmable
 - a) AND array
 - b) OR array
 - c) Both are programmable
 - d) Both are non programmable

8. FPGA consists of an array of
 - a) Configurable logic blocks
 - b) Look up tables
 - c) PLD
 - d) PROM
9. Which component is used to provide a convenient method to store and share declarations that are common for many design units?
 - a) Function
 - b) Procedure
 - c) Package
 - d) Test Bench
10. All statements written under 'Process' will be executed
 - a) Sequentially
 - b) Consecutively
 - c) Based on the priority of case statements
 - d) Based on the library

PART B (10 x 2 = 20 Marks)

11. What are the various CMOS fabrication technologies?
12. Write the NMOS transistor current equation for various regions.
13. What is meant by stick diagram? Draw the stick diagram of an OR gate.
14. Draw the schematic of NMOS inverting and non inverting super buffers.
15. Write short notes on design rules.
16. Draw the circuit diagram of 4 x 1 mux implemented in pass transistor logic.
17. Mention the various programmable devices available for implementing logic functions.
18. Compare PLD and FPGA.
19. Write the VHDL code for NAND gate.
20. What are the various operators in VHDL programming?

PART C (5 x 14 = 70 Marks)

21. a) (i) Explain the working principle of NMOS device. (6)
 (ii) With a neat diagram explain the various steps involved in NMOS fabrication (8)
 (OR)
 b) (i) Explain the second order effects of MOS transistor in detail.
22. a) (i) Derive the pull up to pull down ratio of NMOS inverter driven by one or more pass transistor. (10)
 (ii) What are the various forms on NMOS pull up? (4)
 (OR)
 b) (i) Explain the DC characteristics of CMOS inverter in detail. (10)

- (ii) Implement the following function using pass transistor and transmission gate logic (4)
- $$F = \bar{a} b + c$$
- $$F = a \text{ xor } b$$

23. a) (i) Draw the circuit diagram of barrel shifter implemented in pass transistor logic and explain the working with an example. (10)
- (ii) Write short notes on clocking. (4)

(OR)

- b) (i) Design a four bit even Parity generator. Realize it in stick diagram. (8)
- (ii) Write short notes on Dynamic CMOS logic. (6)

24. a) Explain the implementation of a logic function using NMOS NOR-NOR PLA and NMOS NAND-NAND PLA.

(OR)

- b) What is an FPGA? Explain in detail and give the advantages of FPGA over ASIC.

25. a) (i) Write a VHDL program for full adder using half adder. (7)
- (ii) What are the various data types used in VHDL programming? Explain each with an example. (7)

(OR)

- b) (i) Write a VHDL program for 3 bit up counter using case statement. (8)
- (ii) Write a VHDL code for D flip flop. (6)
