



M.E., DEGREE EXAMINATIONS: APRIL 2015

(Regulation 2013)

Third Semester

APPLIED ELECTRONICS

P13AETE04: DSP Integrated Circuits

Time: Three Hours

Maximum Marks: 100

Answer all the Questions:-

PART A (10 x 2 = 20 Marks)

1. List any two fixed point number representations.
2. How a basic shift-accumulator could be improved?
3. What are the advantages of digital signal processing?
4. Compare the computational complexities of DFT and FFT.
5. Sketch the time-domain and spectrum of a generic decimator.
6. How is an IIR filter specified?
7. State any two VLSI process technologies.
8. What are the advantages of CMOS technology?
9. Differentiate between systolic and wave front arrays.
10. State the memory bottleneck equation.

Answer any FIVE Questions:-

PART B (5 x 16 = 80 Marks)

Q.No:11 is Compulsory

11. Illustrate with examples, the redundant and residue number systems.
12. i) Describe any **one** adaptive DSP algorithms using neat block diagram. (8)
ii) Using signal flow diagram, explain 8-point, DIT FFT algorithm. (8)

13. i) Describe any **two** structures used for FIR filter. (8)
ii) What are finite word length effects? Explain. Also, state how the same (8)
could be minimized.
14. i) Explain any **two** VLSI process technologies used. (8)
ii) Comment on the future trends in VLSI and CMOS technologies. (8)
15. Illustrate the working of systolic array with a neat diagram.
16. Explain how shared memory architectures are designed with a neat block diagram. Also, highlight how the salient features are optimized.
