KUMARAGURU college of technology
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Register Number:……

M.E DEGREE EXAMINATIONS: JUNE 2015

(Regulation 2014)

Second Semester

APPLIED ELECTRONICS

P14AET203: ASIC Design

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. The important steps in FPGA design flow are: [K_2]

   1. Describe 2. Simulate 3. Configure 4. Synthesize. The correct order of design flow is

   a) 1-2-3-4 b) 4-3-2-1

   c) 1-2-4-3 d) 4-2-3-1

2. Channel-less gate array ASIC is an example of [K_1]

   a) Full custom ASIC b) Semi-custom ASIC

   Programmable ASIC d) Gate-array based ASIC

3. The smallest programmable element is [K_2]

   a) EPROM b) Anti-fuse

   c) EEPROM d) SRAM

4. Match the type of device given in List I with the programming technology listed in List II [K_3]

List I	List II
A. ACT1	i. EEPROM
B. XC4000	ii. Anti-fuse
C. MAX 5000	iii. SRAM
D. FLEX8000	iv. EEPROM

	A	B	C	D
a)	i)	ii)	ii)	iv)
b)	iii)	iv)	iii)	i)
c)	iv)	iii)	i)	ii)
d)	ii)	i)	iv)	iii)

5. Assertion (A): **Clock is an important input signal.** [K4]

Reason (R): **Meta-stability occurs due to clock time violations.**

a) Both A and R are individually true and R is not the correct explanation of A

b) Both A and R are individually true and R is the correct explanation of A

c) A is true and R is false

d) A is false and R is true

6. The power dissipation capability of ceramic package is [K1]

a) 10W

b) 1W

c) 2W

d) 0.5W

7. The type of connections boxes used in fast track in Altera FPGA are [K_1]

a) A and B

b) Row and Column boxes

c) PIP and PSM

d) A, B and C

8. Altera FLEX devices have an row, column aspect ratio of [K_1]

a) 1:1

b) 1:10

c) 1:2

d) 1:100

9. 'Sim' bits used for logic verifications are [K_1]

a) '0', '1', and 'X'

b) '0' and '1'

c) 'X' and 'z'

d) 0', '1', 'X' and 'z'

10. Which of the following is true - [K_2]

a) Event and transaction are unrelated

b) An event may cause a transaction

c) An event always results in transaction.

d) A transaction is necessary for an event

PART B (10 x 2 = 20 Marks)

11. What is data path? [K_1]
12. Define cell importance. [K2]
13. Cite any two examples of PREP benchmark circuits [K_1]
14. Compare SPARTAN and VIRTEX series FPGAs [K_4]
15. Define noise margin. [K_1]
16. Relate upset with respect to input. [K_1]
17. Differentiate segmented and non-segmented routing. Give an example for each. [K_2]
18. Correlate fast track lines in Altera with respect to interconnect. [K_4]
19. Illustrate design verification methodology. [K_3]
20. Evaluate the capabilities and limitations of logic simulation. [K_4]

PART C (10 x 5 = 50 Marks)

21.	Illustrate the architecture of gate array based ASIC devices	[K_3]
22.	Given Boolean equation Z = (AB + CD +E)', interpret switch level structure.	[K_2]
23.	Demonstrate, using Shannon's expansion theorem, how the Boolean function given by F = A.B + B'.C + D is implemented on ACT1 FPGA.	[K_3]
24.	Illustrate how logic expanders are used in Altera FPGAs.	[K_3]
25.	Analyze CMOS-CMOS logic compatibility.	[K_4]
26.	Describe the Xilinx XC4000 IOB architecture.	[K_2]
27.	Compare Altera MAX and Xilinx EPLD devices.	[K_3]
28.	Generalize the routing architecture used in Altera MAX devices.	[K_3]
29.	Compare different types of logic simulations.	[K_3]
30.	Categorize different delay models used for simulation.	[K_4]

PART D (2 x 10 = 20 Marks)

31.	Illustrate event driven simulation with neat schematics. Also, highlight the importance of delta delays.	[K_3]
32.	Analyze the design and synthesis of 3-bit comparator/Mux circuit. Demonstrate the design starting from basic 1-bit comparator.	[K_4]

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