KUMARAGURU
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Register Number: ……

B.E DEGREE EXAMINATIONS: JUNE 2015

(Regulation 2013)

Second Semester

COMPUTER SCIENCE AND ENGINEERING

U13CST201: Digital Systems And Design

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. Simplify the expression Y=(A'+B)(A+B)

   a) 0 b) B

   c) A d) BA

2. Find X in the following: $(011010)_2 = (X)_{16}$

3. It is desired to route data from many registers to one register. The device needed is _____

   a) Encoder b) Demultiplexer

   c) Multiplexer d) Decoder

4. Addition of 8 and 4 in BCD code is ----------

5. In a positive edge triggered JK flip-flop, a low J and low K produces

   a) No change b) Low state

   c) High state d) Toggle

6. Number of flipflops required to design Mod – 10 counter is -----

7. Essential hazard is avoided by _____

   a) Adding feedback b) Adding delay elements

   c) Edge triggering d) Redundant grouping

8. In moore model the output is a function of _____

9. In EPROM, information is erased by means of _____

   a) Infrared b) Ultraviolet light

   c) Electric d) All the above

10. The Fan-in of a logic gate refers to the number of _____

PART B (10 x 2 = 20 Marks)

(Not more than 40 words)

11. Define duality property with an example
12. Convert the following into gray code: a) 110101 b)100111
13. Design 2 X 4 Decoder
14. Design Half Adder Circuit
15. Distinguish between edge triggered and level triggered flipflops
16. What is race around condition? How it is rectified?
17. Compare Mealy and Moore model of sequential circuits.
18. Differentiate between synchronous and asynchronous counters.
19. What is PLA and how it is different from PAL?
20. Define CMOS.

PART C (5 x 14 = 70 Marks)

(Not more than 400 words)

Q.No. 21 is Compulsory

21. (i) Explain SR and JK flipflop with logic diagram, characteristic table. (7)

    (ii) Design Mod -4 synchronous counter (7)

22. a) Simplify the following function using tabulation method.

    $F(x1,x2,x3,x4,x5) = \sum (0,2,4,5,6,7,8,10,14,17,18,21,29,31) + \sum d(11,20,22)$

    (OR)

    b) (i) Simplify the boolean function using K-map $Y = \Sigma m (7,9,10,11,12,13) + d(14,15)$ (8)

    (ii) Simplify the Boolean function using algebraic method. (6)

    a) Y= A'B'C'+A'BC'+AB'C'+ABC' b) F=xy+x'z+yz

23. a) (i) Design code converter to convert gray to binary (7)

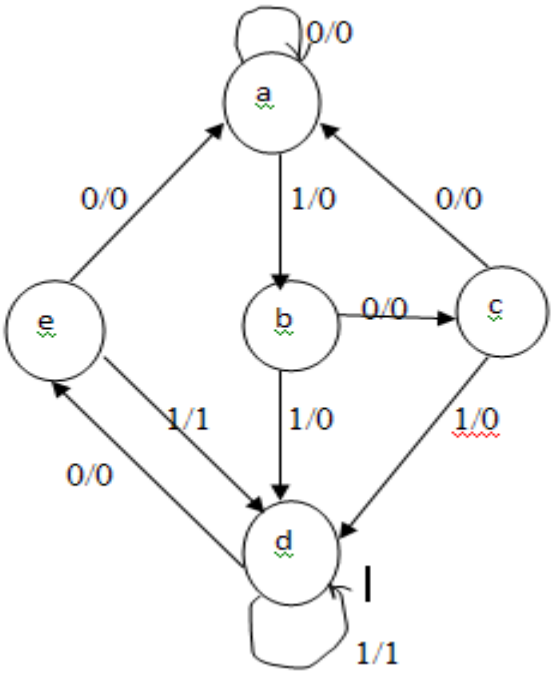
    (ii) Design 4 bit parallel Binary Adder (7)

    (OR)

    b) (i) Design and Explain 4 bit Carry look ahead generator (7)

    (ii) Design 3 bit even parity generator and checker. (7)

24. a) Design a sequential circuit for the following state diagram using JK flipflops.



(OR)

b) (i) Draw the circuit diagram of SISO and PISO shift register and explain with an example. (7)

(ii) Design Hazard free circuit for the function F(A,B,C,D) = ∑(0,2,6,7,8,10,12) (7)

25. a) (i) Implement the following boolean function with PLA (10)

$A(x, y, z) = \Sigma m\ (1, 2, 4, 6)$
$B(x, y, z) = \Sigma m\ (0, 1, 6, 7)$
$C(x, y, z) = \Sigma m\ (2, 6)$

(ii) Write short note on FPGA (4)

(OR)

b) (i) Draw the circuit of a basic CMOS cell. Explain the working of the same. (7)

(ii) Implement the following Boolean function with PROM (7)

F1(A0,A1) = ∑(1.2)

F2(A0,A1) = ∑(0,1,3)

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