KUMARAGURU
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Register Number: …….

B.E DEGREE EXAMINATIONS: MAY 2015

(Regulation 2013)

Forth Semester

ELECTRICAL AND ELECTRONICS ENGINEERING

U13EET404**:** Digital Electronics

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. Which of the following is the fastest logic
   a) TTL b) ECL
   c) CMOS d) LSI
2. The 2's complement of the number 1101101 is ……..
3. Data can be changed from special code to temporal code by using
   a) Shift registers b) counters
   c) Combinational circuits d) A/D converters
4. If the input to T-flipflop is 100 Hz signal, the final output of the three T-flipflops in cascade is ……..
5. DeMorgan's first theorem shows the equivalence of
   a) OR gate and Exclusive OR gate b) NOR gate and Bubbled AND gate
   c) NOR gate and NAND gate d) NAND gate and NOT gate
6. The storage element for a static RAM is the ……..
7. Which gate is best used as a basic comparator?
   a) NOR b) OR
   c) Exclusive-OR d) AND
8. The inverter can be produced with how many NAND gate is ……..
9. The expansion of FPGA is_____
   a) Field process Gate array b) Flexible programmable gated array
   c) Fixed programmable group array d) Field programmable gate array
10. How is a J-K flip-flop made to toggle is……..

PART B (10 x 2 = 20 Marks)

(Not more than 40 words)

11. State De Morgan's theorem.
12. Draw an active-high tri-state buffer and write its truth table.
13. Define fan-in.
14. Draw the flow diagram of Gray to Binary conversion.
15. Convert (367)10 in to Excess 3 code.
16. What is race around condition?
17. Explain the write operation with example.
18. What is meant by programmable counter? Mention its application.
19. What is PAL? How does it differ from PLA.
20. List the advantages of FPGA.

PART C (5 x 14 = 70 Marks)

(Not more than 400 words)

Q.No. 21 is Compulsory

21. Simplify the following Boolean function by using Quine-Mcclusky method
F (A,B,C,D) $\sum$= (0,2,3,6,7,8,10,12,13)

22. a) Using the K-map method obtain the minimal SOP & POS expression for the function
F (X,Y,Z,W) =$\sum$ (1,3,4,5,6,7,9,12,13)

(OR)

b) Design a carry look ahead adder with necessary diagrams.

23. a) Draw and explain the block diagram of a 4-bit serial adder to add the contents of two registers.

(OR)

b) (i) Explain the operations of 4 Bit magnitude comparator. (10)

(ii) Explain the concepts of even parity checker (4)

24. a) (i) Draw the 4- bit johnson counter & explain the operation (7)

(ii) Draw a 8-bit SIPO shift register & explain the operation. (7)

(OR)

b) Design a negative-edge triggered ‘T flipflop

25. a) Write short notes on the following giving one example of each

(i) State table (ii) State Diagram

(iii) Cycle (iv) Races

(OR)

b) Design a combinational circuit using a ROM. The circuit accepts a three bit number and outputs a binary number equal to the square of the input number.

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