KUMARAGURU
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B.TECH DEGREE EXAMINATIONS: MAY 2015

(Regulation 2013)

Third Semester

INFORMATION TECHNOLOGY

U13ITT302: Digital Systems And Design

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. Using 10's complement ,subtract$(3250\text{-}72532)_{10}$
   a) 69282 b) -69282
   c) 62829 d) 69829
2. The Octal equivalent of $(0.513)_{10}$ is …….
3. A combinational circuit that selects binary information from one of many input lines and direct it to a single output line
   a) Multiplexer b) De multiplexer
   c) Binary De multiplexer d) Binary Multiplexer
4. A…….. is a combinational circuit that compares two numbers ,A and B, and determine their relative magnitudes.
5. SR latch is also called as
   a) Indirect-Coupled JK Flip Flop b) Direct-coupled JK Flip Flop
   c) Direct-coupled RS Flip Flop d) Indirect –coupled RS Flip Flop
6. Synchronization is achieved by a timing device called a …… which generates a periodic train of clock pulses.
7. A sequential circuit that goes through a prescribed sequence of states upon the application of input pluses is called as _____
   a) Encoder b) Counter
   c) Decoder d) Ripple counter
8. A binary counter with a reverse count is called a ……..
9. An interrupt system that establishes a priority over the various sources to determine which condition is to be serviced first when two or more requests arrive simultaneously

a) Parity Generator
b) Parity checker
c) Priority Interrupt
d) Priority checker

10. ECL stands for……..

PART B (10 x 2 = 20 Marks)

11. State and prove Demorgan's law.
12. Simplify the given Boolean Expression F=x'+xy+xz'+xy'z.
13. Design a 3 bit even parity generator.
14. List out Various applications of Multiplexer.
15. Differentiate Moore and Mealy state machines.
16. How a D Flip Flop is converted to a T Flip Flop.
17. Design a 3-bit ring counter and find the mod of the designed counter.
18. What is the characteristic equation of JK Flip Flop?
19. Differentiate PLA and PAL.
20. Calculate the Base current with values of V_i=5V, V_{BE}=0.7 and R_B=22k ohms.

PART C (5 x 14 = 70 Marks)

Q. No . 21 is Compulsory

21. (i) Simplify the Boolean Function: (6)
F(A,B,C,D,E)=∑(0,2,4,6,9,11,13,15,17,21,25,27,29,31)

(ii) Determine the prime-implicants of the Function: (8)
F(w, x ,y ,z)=∑(1,4,6,7,8,9,10,11,15)

22. a) (i) Implement the following function with a multiplexer: (7)
F(A,B,C,D)=∑(0,1,3,4,8,9,15)

(ii) Explain about Magnitude comparator with necessary diagrams (7)

(OR)

b) (i) Explain the operation of BCD adder (8)

(ii) Design a Full adder using two half adders and OR gate (6)

23. a) Design a 3-bit binary counter by providing the excitation table and logic diagram for it.

(OR)

b) Explain the master-slave and clocked master slave flip flop with necessary details.

24. a) What is a Hazard? What are the types of Hazard? Check whether the following circuit contains the hazard or not Y=x1x2+x2'x3.If the hazard is present, demonstrate its removal.

(OR)

b) (i) Construct a 4-bit binary ripple counter with logic and timing diagram (8)

(ii) Compare Asynchronous counter and synchronous counter (6)

25. a) (i) Explain about Transistor-Transistor Logic with necessary diagrams (8)

(ii) Briefly explain about EPROM and EEPROM technology (6)

(OR)

b) (i) Implement the following functions with 3 inputs,3 product terms and 2 outputs PLA F1=AB'+AC+A'BC',F2=(AC+BC)' (7)

(ii) Explain about different addressing modes with examples (7)

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