KUMARAGURU
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Register Number: …….

B.TECH DEGREE EXAMINATIONS: MAY 2015

(Regulation 2013)

Fourth Semester

INFORMATION TECHNOLOGY

U13ITT405: Computer Architecture

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. Computers use addressing mode techniques for
   a) giving programming versatility to the user by providing facilities as pointers to memory counters for loop control
   b) to reduce no. of bits in the field of instruction
   c) specifying rules for modifying or interpreting address field of the instruction
   d) All the above
2. Program counter contains ----------.
3. When a program generates an access request to a page that is not in the main memory, a ------- is said to have occurred
   a) Page hit
   b) Page frame
   c) Page fault
   d) Page block
4. In virtual memory, address generated by the processor is called as ----------
5. Multiply rule for floating-point numbers states that
   a) Add the exponents and subtract 127
   b) Subtract the exponents and add 127
   c) Subtract the exponents and subtract 127
   d) Add the exponents and add 127
6. A 4 bit Carry-look ahead adder has ----- gate delays for all carry bits and ----- gate delays for all sum bits
7. A pipelined processor may process each instruction in four steps as follows
   a) F,D, EXE, WB
   b) D,F,EXE,WB
   c) F,D,WB,EXE
   d) F,WB,D,EXE

8. Any condition that causes the pipeline to stall is called a ----------.
9. SCSI stands for
   a) Smart Computer System Interface
   b) Smart Computer Small Interface
   c) Small Computer Smart Interface
   d) Small Computer System Interface
10. The device that is allowed to initiate data transfers on the bus at any given time is called the ------.

PART B (10 x 2 = 20 Marks)

(Not more than 40 words)

11. Calculate the program execution time for executing a total of 400 machine language instructions in a program. Assume that on an average there are 8 basic steps needed to execute 1 machine instruction and each basic step is completed in 1 clock cycle. The clock rate is 800 cycles/second
12. Compare Big-endian and Little-endian method of assigning byte addresses.
13. If the cache memory of capacity 1K words uses direct mapping with a block size of 4 words, how many blocks can the cache have?
14. Illustrate the working of LRU replacement algorithm.
15. What do you mean by Chopping?
16. Obtain the Booth multiplier recoding table.
17. What do you mean by speculative execution?
18. What is the difference between horizontal and vertical organization of microinstructions?
19. Compare PCI and SCSI bus standards.
20. What is the difference between centralized and distributed bus arbitration.

PART C (5 x 14 = 70 Marks)

(Not more than 400 words)

Q.No. 21 is Compulsory

21. What are interrupts? Discuss about the hardware and software needed to support them.

22. a) Explain data transfer between processor and the I/O devices. Illustrate with an example.

(OR)

b) With suitable examples, explain various addressing modes.

23. a) Explain how a virtual address generated by a processor is translated to physical address.

(OR)

b) (i) Suppose that a cache with 8-word blocks is used and that the hardware has the following properties: It takes 1 clock cycle to send an address to the main memory. The first word is accessed in 9 clock cycles and subsequent words of the block are accessed in 6 clock cycles per word. One clock cycle is needed to send one word to the cache. Calculate the time needed to load the desired block into the cache if (10)

(i) Single memory module is used.

(ii) Memory is constructed as four interleaved modules.

(ii) Discuss about Flash memory. (4)

24. a) Explain about Bit-pair recoding of multipliers and multiply 5 ,(-8) using Bit-pair recoding of multipliers.

(OR)

b) Explain Restoring and Non-Restoring methods for division of integer numbers with an example for each method.

25. a) Explain about Hardwired control method of generating control signals with examples.

(OR)

b) Explain about delayed branching and dynamic branch prediction.

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