B.E DEGREE EXAMINATIONS: MAY 2015

(Regulation 2013)

Fourth Semester

MECHATRONICS ENGINEERING

U13MCT405:Digital Electronics

Time: Three Hours   **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1.   Which of the following expressions is in the sum-of-products (SOP) form?

    a) $(A + B)(C + D)$ b) $(A)B(CD)$

    c) $AB(CD)$ d) $AB + CD$

2.   A major advantage of ECL logic over TTL and CMOS is _____.

3.   To implement the expression $A\bar{B}CD + AB\bar{C}D + ABC\bar{D}$, it takes one OR gate and _____.

    a)   three AND gates and three inverters   b)   three AND gates and four inverters

    c)   three AND gates   d)   one AND gate

4.   Assume you have A, B, C, and D available but not their complements. The minimum number of 2-input NAND gates required to implement the equation $X = A\bar{B} + B\bar{C}$ is _____.

5.   A BCD counter is a _____.

    a)   binary counter   b)   full-modulus counter

    c)   decade counter   d)   divide-by-10 counter

6.   Determine the output frequency for a frequency division circuit that contains 12 flip-flops with an input clock frequency of 20.48 MHz.

7.   The group of bits 11001 is serially shifted (right-most bit first) into a 5-bit parallel output shift register with an initial state 01110. After three clock pulses, the register contains _____.

    a)   01110   b)   00001

    c)   00101   d)   00110

8.   With a 200 kHz clock frequency, eight bits can be serially entered into a shift register in _____.

9. How many address bits are needed to select all memory locations in the 2118 16K $\times$ 1 RAM?

    a) 8   b) 10

    c) 14   d) 16

10. The _____ is the most popular standard logic device family today.

PART B (10 x 2 = 20 Marks)

(Not more than 40 words)

11. Convert $(101011)_2$ to gray code.

12. Write the characteristics of TTL

13. Define parity generator.

14. Draw the block diagram of n-bit comparator.

15. What is the limitation of half adder?

16. Differentiate Combinational and Sequential Circuits.

17. Write short note on basic bi-stable element

18. What is the minimum number of flip-flops needed to design a counter of modulus 60?

19. Mention the two types of erasable PROM.

20. Define NOR Flash memory

PART C (5 x 14 = 70 Marks)

(Not more than 400 words)

Q.No. 21 is Compulsory

21. Derive Excess-3 code from BCD codes using K-map simplification. Explain with truth table and logic diagram.

22. a) (i)   Implement the Boolean function using 8:1 multiplexer.   (10)

    $$F = (A, B, C, D) = A\overline{B}D + \overline{A}CD + \overline{B}C\overline{D} + A\overline{C}D$$

    (ii) Implement Boolean function F = $\sum$ m (1, 2, 3, 7) using 3:8 decoder   (4)

(OR)

    b) Draw the logic diagram of carry look ahead adder and explain its operation.

23. a) Realize D flip-flop using JK flip-flop

            (i) Write the characteristic table for D flip-flop

            (ii) Write the excitation table for JK flip-flop

            (iii) Determine the expression of inputs J and K using K-map

            (iv) Draw the flip-flop conversion logic diagram

(OR)

b) (i) What is race round condition? How is it avoided? (6)

(ii) Draw the schematic diagram of master-slave JK Flip-flop and discuss how it prevents race around condition. (8)

24. a) Using JK flip-flops, design a synchronous counter which counts in the sequence, 000, 001, 010, 011, 100, 101, 110, 111, 000.

(OR)

b) (i) Explain in detail about the types of shift registers with neat sketch. (10)

(ii) Compare Moore and Mealy circuits. (4)

25. a) (i) Design a Full Adder using a suitable PROM (6)

(ii) Implement the given functions using PROM (16) F1 = $\sum$ (0, 1, 3, 4, 6, 7) F2 = $\sum$ (1, 2, 3, 5) (8)

(OR)

b) (i) Write short note on semiconductor memories. (6)

(ii) Categorize RAM and ROM and explain in detail. (8)

∗∗∗∗∗∗∗∗∗∗∗∗∗